MODEL	REV	CHANGE LIST
TW3A M/B	3A	First Release 31T3MB0033 (E200601-0720) 2006/1/10
	3B	E200601-5311 2006/2/8

Model / Page	TW3A M/B From	To
1	3A	
2	3A	
3	3A	
4	3A	
5	3A	
6	3A	
7	3A	
8	3A	
9	3A	
10	3A	
11	3A	
12	3A	
13	3A	
14	3A	3B
15	3A	
16	3A	
17	3A	
18	3A	
19	3A	3B
20	3A	
21	3A	
22	3A	
23	3A	3B
24	3A	
25	3A	
26	3A	3B
27	3A	3B
28	3A	
29	3A	3B
30	3A	
31	3A	
32	3A	3B
33	3A	3B
34	3A	
35	3A	3B
36	3A	3B
37	3A	
38	3A	
39	3A	
40	3A	
41	3A	3B
42	3A	
43	3A	3B
44	3A	
45	3A	
46	3A	
47	3A	
48	3A	

PROJECT : TW3A
Quanta Computer Inc.

PROJECT: TW3A	ASSY P/N:31TW3MB0033	TITLE:	DOC NO:204
APPROVED BY : Johnson Hsu	DRAWING BY : Tony Huang	VER:3B	DATE :02/08/2006 SHEET 1

TW3A- DESIGN

31TW3MB00XX

1

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

RUN POWER SW PG 43

AC/BATT CONNECTOR PG 40

BATT CHARGER PG 40

Yonah/Merom
31W/35W
(478 Micro-FCPGA)
PG 4,5

CPU VR PG 37

DC/DC +3VSUS +5VSUS PG43

DC/DC +3VPCU +5VPCU PG38

DC/DC +1.05V +1.5V PG37

CLOCKS ICS954206 PG 3

FSB 133MHZ

DDRII VR PG 39

DDRII-SODIMM1 PG 16,17

DDRII-SODIMM2 PG 16,17

DDRII 667mhz

DDRII 667mhz

Calistoga PM
945PM
Integraded VGA Function
1466 BGA
PG 6,7,8,9,10,11

PCI-Express 16X

nVIDIA
NV72M/MV
(64 Bit B/W)
DDRII
16M*16(128MB)
32M*16(256MB)
(Bank*4)
PG 18~21

DC/DC VGA CORE PG42

LVDS(2 Channel)

Panel Connector PG 22

TVOUT

S-Video PG 35

VGA

VGA,DVI PG 23

DMI interface

SATA - HDD PG 29

PATA - HDD PG 29

Internal ODD CD-ROM PG 29

SATA0

PATA 100

ICH7-M

652 BGA

PG 12,13,14,15

USB2.0 (P0~P7)

USB2.0 (P5)

Bluetooth PG 33

USB2.0 (P0~P1,P4)

USB2.0 I/O Ports PG 26

PCI-E, 1X

LAN 88E8038/88E8055 PG 24

Magnetics PG 25

RJ45 PG 25

PCI-E, 1X

Mini PCI-E Card
PCI Express Mini Card
PG 33

PCI-E, 1X

Express Card x1 NEW CARD PG 33

Azalia

PCI Bus 33MHz

Conexant Audio CX20549-12 PG 30

AUDIO Amplifier PG 31

MDC DAA CX20548-A PG 32

Jack to Speaker PG 31

Audio Jacks PG 30

MODEM RJ 11 PG 32

LPC

TPM1.2 PG 44

KBC PC87541V PG 36

X-Bus

Key Matrix PG 34

Touch Pad PG 34

Flash PG 36

TI PC7402 PG 27

IEEE1394 CONN
3 in 1 Card reader
PG28

Power On
Power Input
LPT PORT
COM PORT
LAN
VGA
Headphone
1394
USB X 2

RQ6
Replicator Daughter Board
USB
PG 35

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	3A

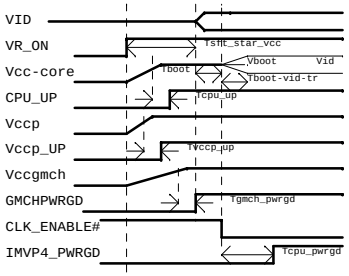
Date: Thursday, June 15, 2006 Sheet 1 of 48

Board Stack up Description

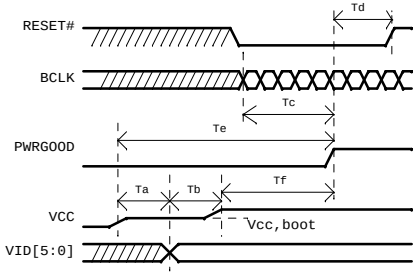
PCB Layers

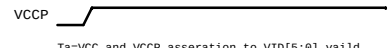
Layer 1		TOP(Component,Other)
Layer 2		Ground Plane
Layer 3		IN1
Layer 4		IN2
Layer 5		Power Plane
Layer 6		IN3
Layer 7		Ground Plane
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



Dothan Power-up Timing Specifications



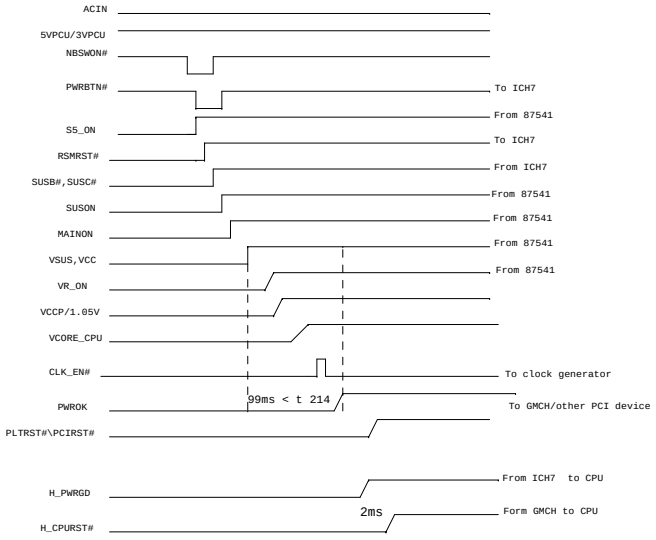


Ta=VCC and VCCP asseration to VID[5:0] vaild
Tb=VID[5:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot vaild to PWRGOOD assertion time

Voltage Rails

Voltage Rails		ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VR_ON 0.726V~0.94V
VCCP	Core voltage for CPU / NB	X				VR_ON
SMDDR_VTERM	0.9V for DDR2 Termination voltage	X				MAINON
RVCC1.5		X	X	X		RVCC_ON
RVCC3		X	X	X		RVCCD
VCC1.5		X				MAIND
VCC2.5		X				MAINON
VCC3		X				MAIND
VCC5		X				MAIND
1.8VSUS		X	X			SUSON
3VSUS		X	X			SUSD
5VSUS		X	X			SUSD
3VPCU		X	X	X	X	VL
5VPCU		X	X	X	X	VL
9VPCU		X	X	X	X	5VPCU

ACIN POWER ON TIMING



Voltage Rails		ON S0~S1	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VRON
GMCH_VTT	Core voltage for GMCH 1.05V	X				MAINON
SMDDR_VTERM	0.9V for DDR II Termination voltage	X				MAINON
SMDDR_VREF	0.9V for DDR II Reference Voltage	X				MAINON
GMCH_1.5V		X				MAINON
1.8VSUS	1.8V for DDR II voltage	X	X			SUSON
+2.5V		X				MAINON
3VPCU		X	X	X	X	VL
3VSUS		X	X			SUSON
+3V		X				MAINON
5VPCU		X	X	X	X	VL
5VSUS		X	X			SUSON
+5V		X				MAINON
VIN	POWER SOURCE	X	X	X	X	

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7402	AD17	REQ2# / GNT2#	PIRQ C/D

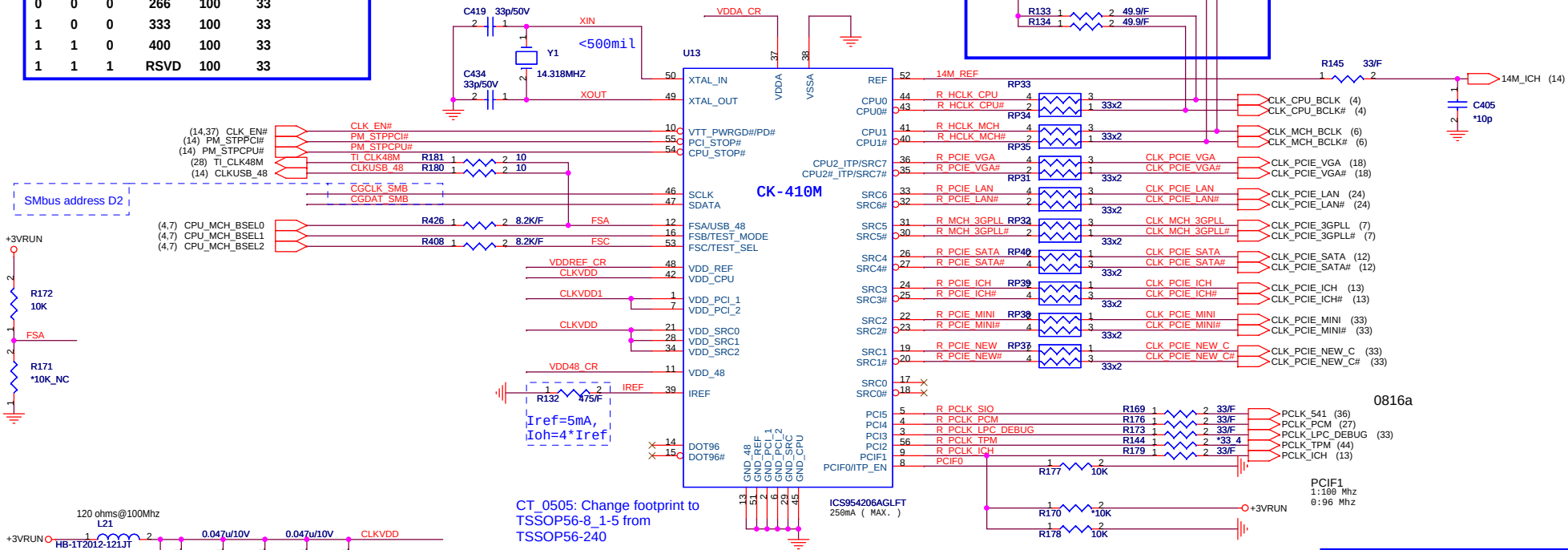
PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	System Information	3A

Date: Thursday, June 15, 2006 Sheet 2 of 48

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

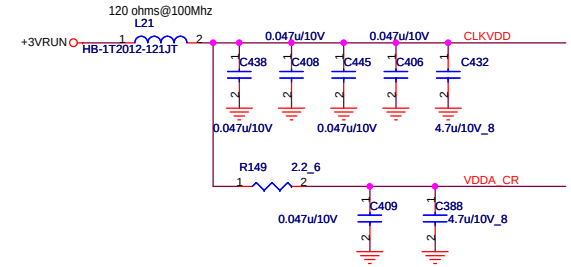
Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

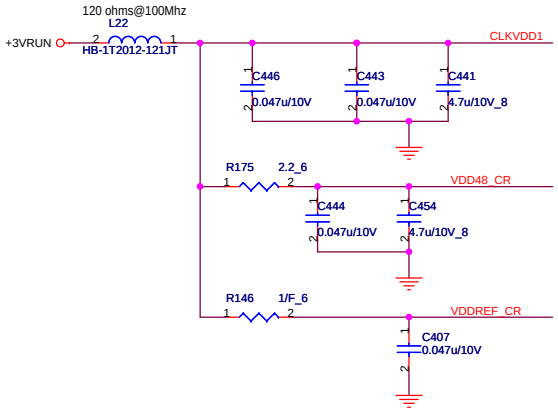


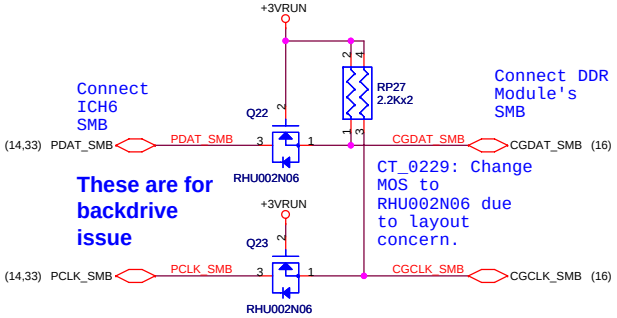
CT_0505: Change footprint to TSSOP56-8_1-5 from TSSOP56-240

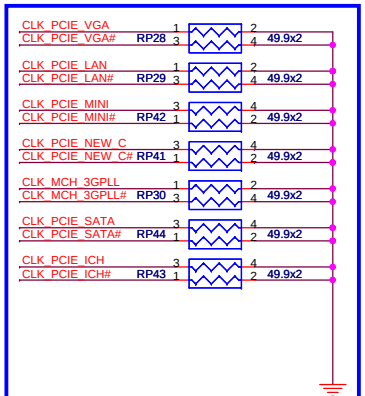
Bypass CAPs need to follow Bypass CAP. Routing Rule, no vias between CAP to CHIPSET VCC Pin or GND.

Tie to VCC (Logic 1) is for ITP using.
Tie to GND (Logic 0) is for PCIE using.







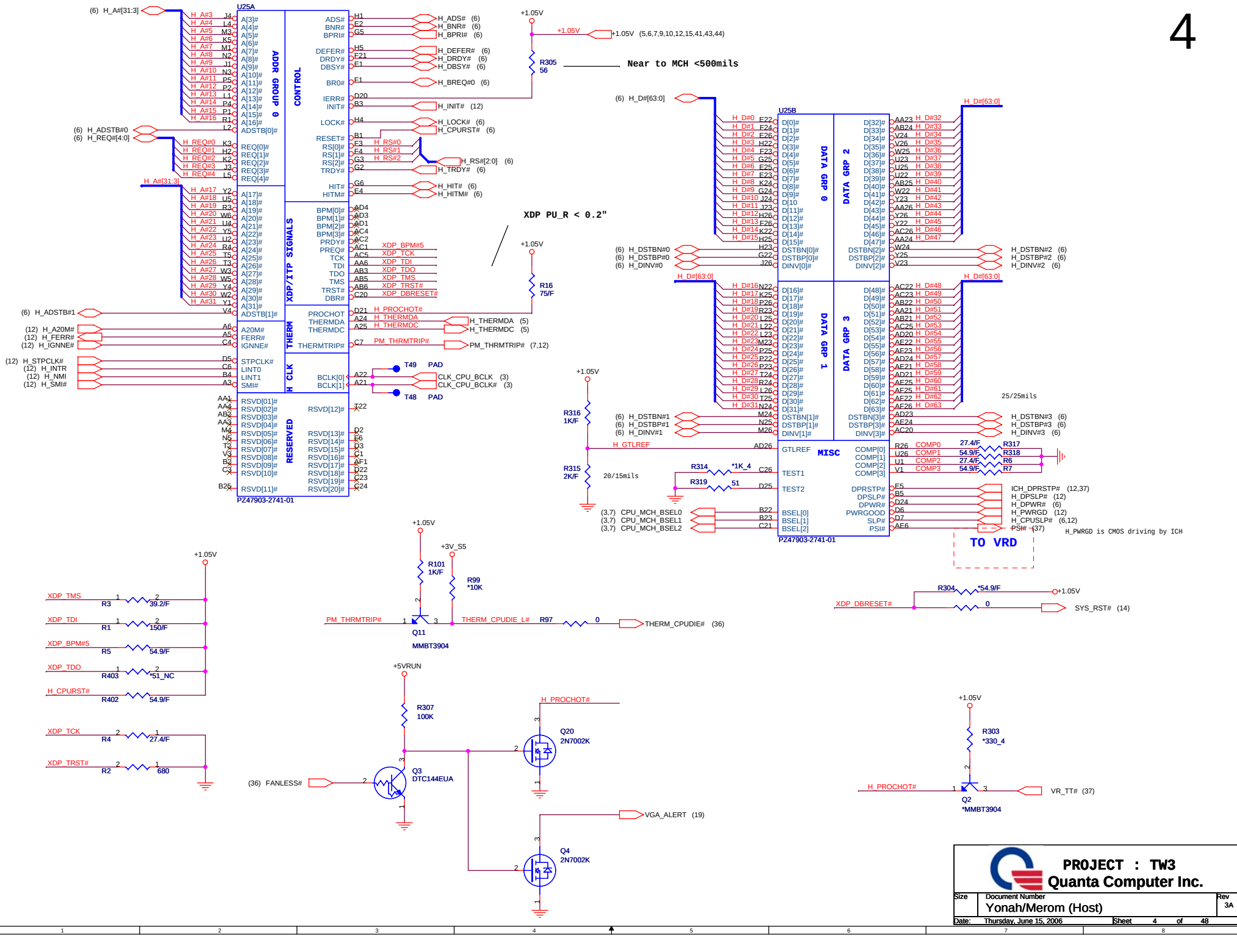


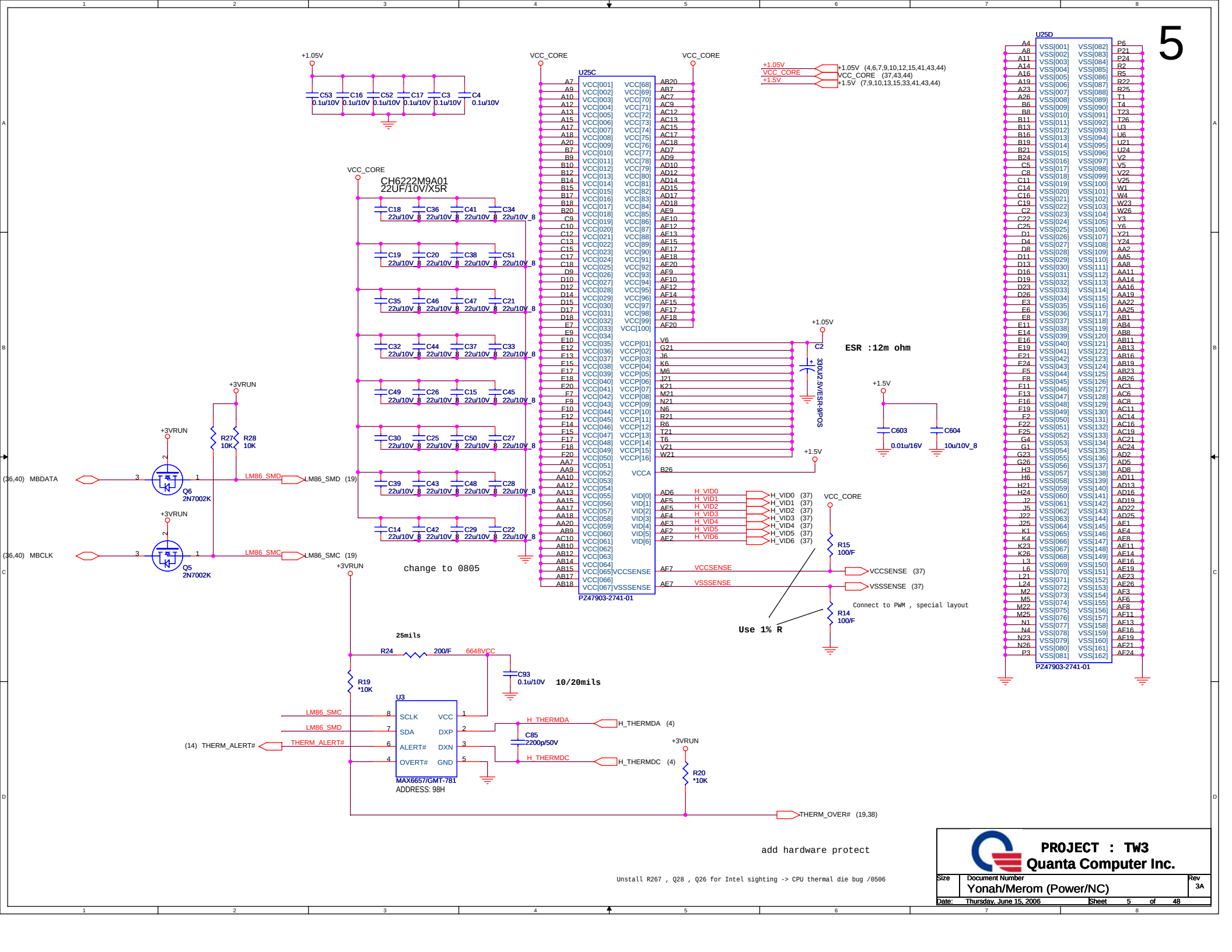
Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR	3A

Date: Thursday, June 15, 2006 Sheet 3 of 48


U25A
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
THERM
H_CLK
RESERVED
PZ47903-2741-01
U25B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
PZ47903-2741-01
XDP PU_R < 0.2"
Near to MCH <500mils
TO VRD
H_PWRGD is CMOS driving by ICH
PROJECT : TW3
Quanta Computer Inc.
Yonah/Merom (Host)
Thursday, June 15, 2006
Sheet 4 of 48


5
+1.05V
VCC_CORE
C53 0.1u/10V
C16 0.1u/10V
C52 0.1u/10V
C17 0.1u/10V
C3 0.1u/10V
C4 0.1u/10V
U25C
PZ47903-2741-01
+1.05V (4,6,7,9,10,12,15,41,43,44)
VCC_CORE (37,43,44)
+1.5V (7,9,10,13,15,33,41,43,44)
U25D
PZ47903-2741-01
CH6222M9A01
22UF/10V/X5R
C18 22u/10V_8
C36 22u/10V_8
C41 22u/10V_8
C34 22u/10V_8
C19 22u/10V_8
C20 22u/10V_8
C38 22u/10V_8
C51 22u/10V_8
C35 22u/10V_8
C46 22u/10V_8
C47 22u/10V_8
C21 22u/10V_8
C32 22u/10V_8
C44 22u/10V_8
C37 22u/10V_8
C33 22u/10V_8
C49 22u/10V_8
C26 22u/10V_8
C15 22u/10V_8
C45 22u/10V_8
C30 22u/10V_8
C25 22u/10V_8
C50 22u/10V_8
C27 22u/10V_8
C39 22u/10V_8
C43 22u/10V_8
C48 22u/10V_8
C28 22u/10V_8
C14 22u/10V_8
C42 22u/10V_8
C29 22u/10V_8
C22 22u/10V_8
C2 330U/2.5V/ESR-9/POS
ESR :12m ohm
C603 0.01u/16V
C604 10u/10V_8
+3VRUN
R27 10K
R28 10K
(36,40) MBDATA
LM86_SMD
LM86_SMD (19)
Q6 2N7002K
(36,40) MBCLK
LM86_SMC
LM86_SMC (19)
Q5 2N7002K
change to 0805
H_VID0 (37)
H_VID1 (37)
H_VID2 (37)
H_VID3 (37)
H_VID4 (37)
H_VID5 (37)
H_VID6 (37)
R15 100/F
R14 100/F
VCCSENSE (37)
VSSSENSE (37)
Connect to PWM , special layout
Use 1% R
25mils
R24 200/F
6648VCC
C93 0.1u/10V
10/20mils
R19 *10K
U3
LM86_SMC
LM86_SMD
(14) THERM_ALERT#
THERM_ALERT#
SCLK
SDA
ALERT#
OVERT#
VCC
DXP
DXN
GND
MAX6657/GMT-781
ADDRESS: 98H
H_THERMDA
H_THERMDA (4)
C85 2200p/50V
H_THERMDC
H_THERMDC (4)
R20 *10K
THERM_OVER# (19,38)
add hardware protect
Unstall R267 , Q28 , Q26 for Intel sighting -> CPU thermal die bug /0506
PROJECT : TW3
Quanta Computer Inc.
Size
Document Number
Yonah/Merom (Power/NC)
Rev 3A
Date: Thursday, June 15, 2006
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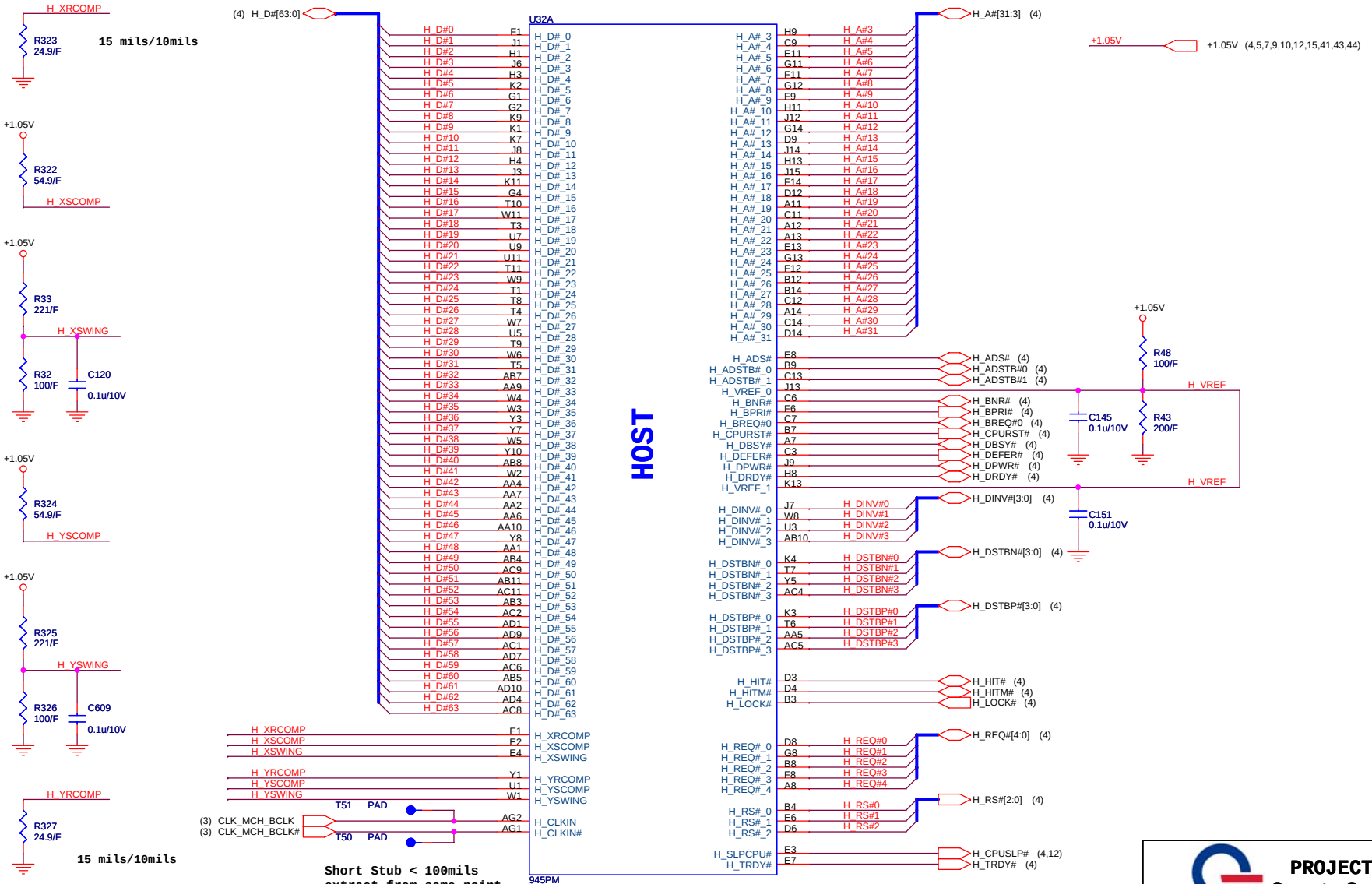
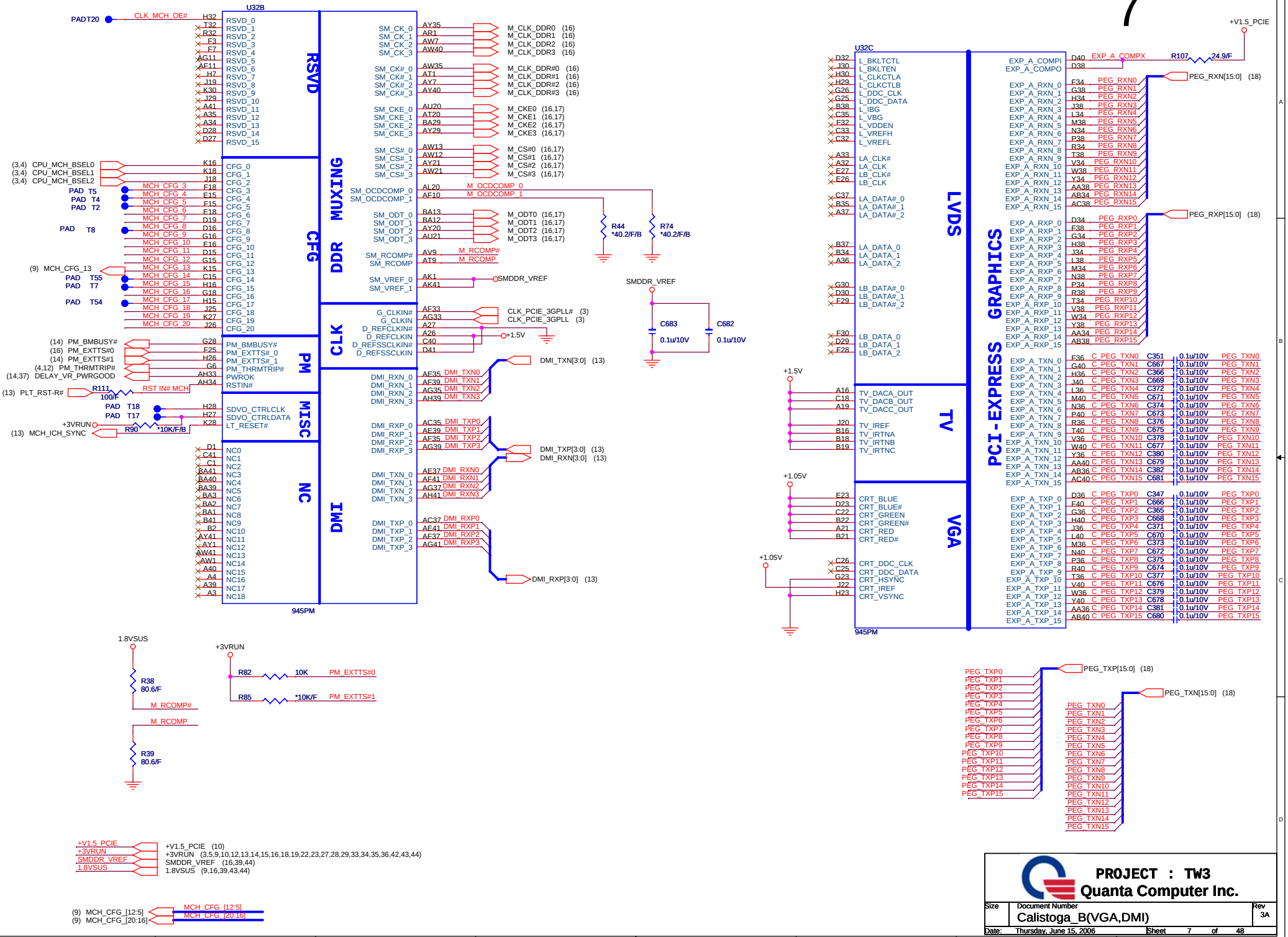
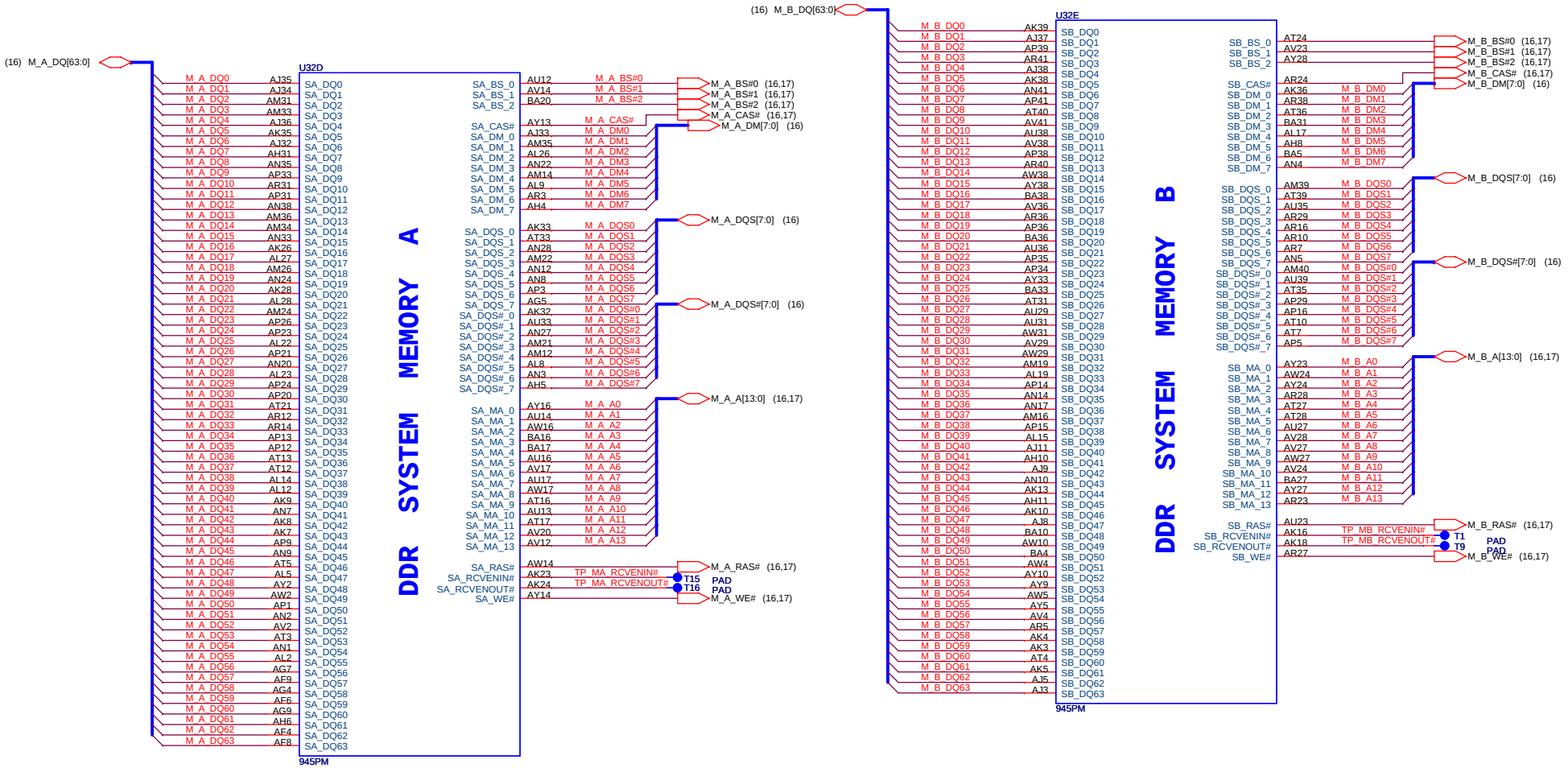


PROJECT : TW3
Quanta Computer Inc.

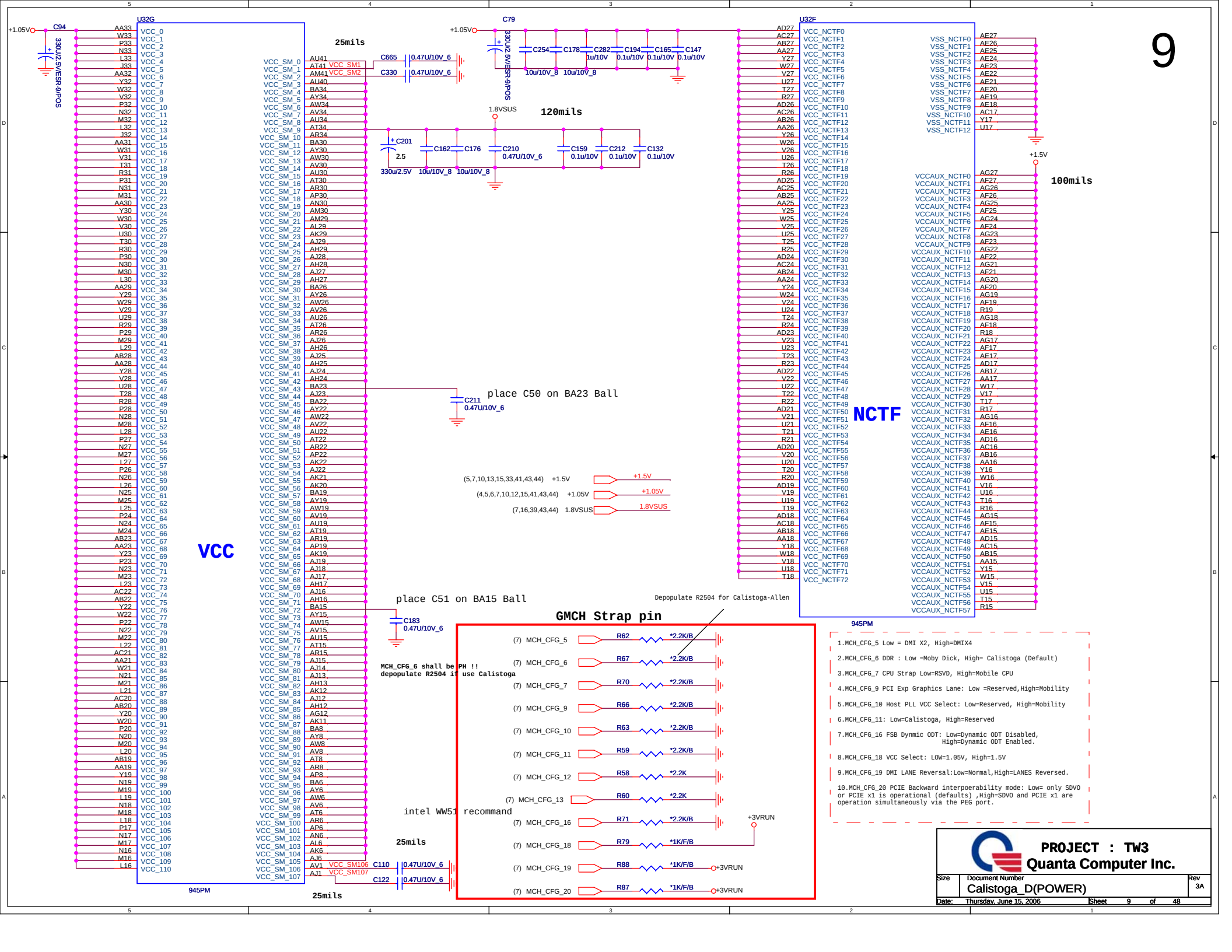
Size	Document Number	Rev
	Calistoga_A(Host)	3A
Date: Thursday, June 15, 2006	Sheet 6 of 48	

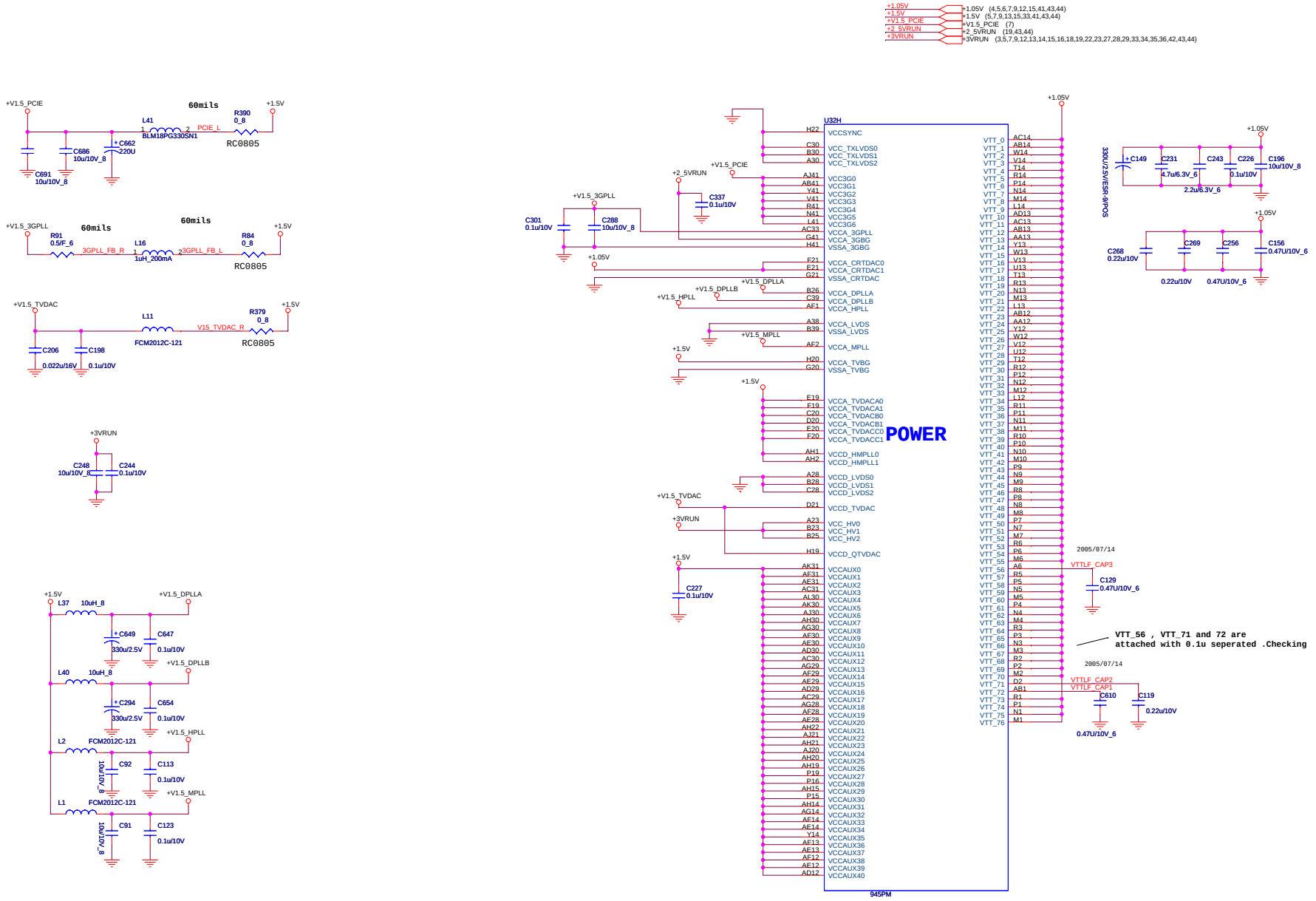


PROJECT :	TW3
Quanta Computer Inc.	
Size	Document Number: Calistoga_B(VGA,DMI) — Rev: 3A
Date: Thursday, June 15, 2006	Sheet 7 of 48

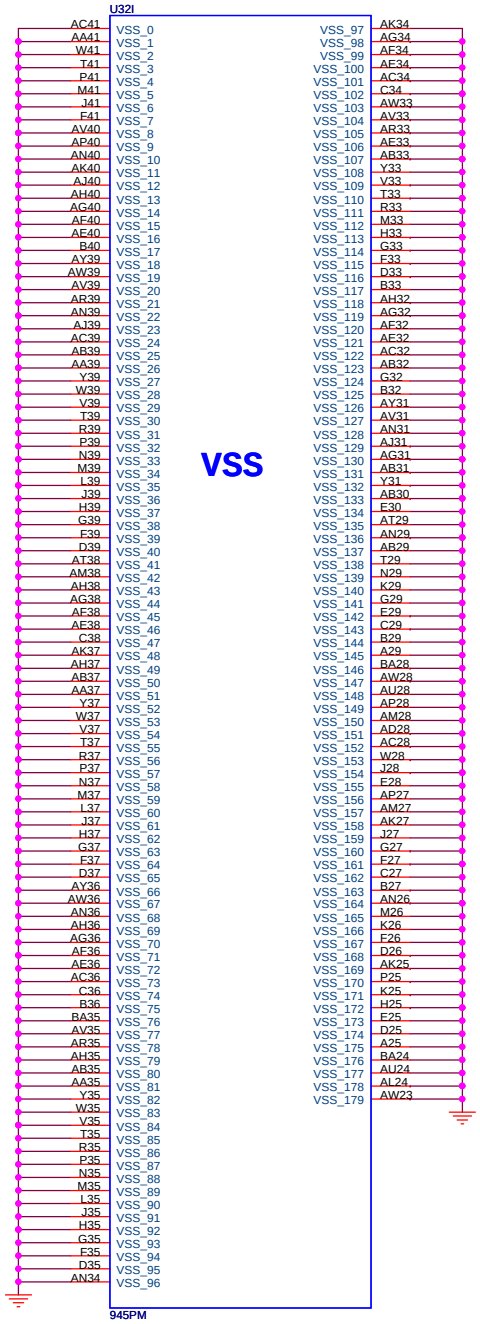


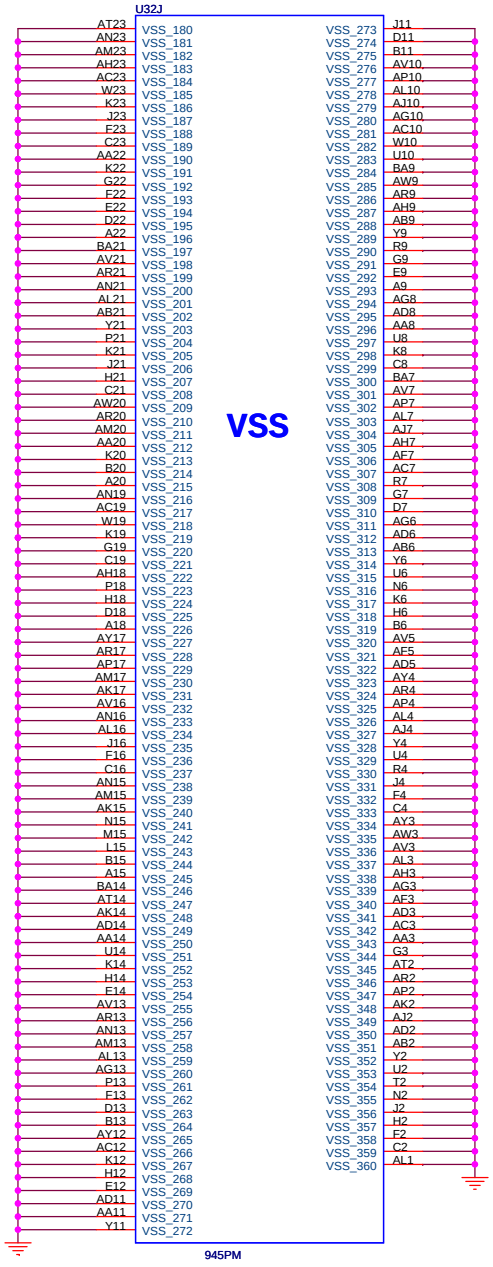
PROJECT : TW3 Quanta Computer Inc.			
Size	Document Number		Rev
	Calistoga_C(DDR)		3A
Date: Thursday, June 15, 2006		Sheet 8 of 48	


9
U32G
VCC
945PM
25mils
120mils
100mils
place C50 on BA23 Ball
place C51 on BA15 Ball
MCH_CFG_6 shall be PH !!
depopulate R2504 if use Calistoga
Depopulate R2504 for Calistoga-Allen
GMCH Strap pin
intel WW51 recommand
U32F
NCTF
945PM
1.MCH_CFG_5 Low = DMI X2, High=DMIX4
2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
6.MCH_CFG_11: Low=Calistoga, High=Reserved
7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.
PROJECT : TW3
Quanta Computer Inc.
Size
Document Number
Calistoga_D(POWER)
Rev 3A
Date: Thursday, June 15, 2006
Sheet 9 of 48



PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number: Calistoga_E(POWER2)	Rev: 3A
Date: Thursday, June 15, 2006	Sheet 10 of 48	





Quanta Computer Inc.	PROJECT : TW3	
Size	Document Number: Calistoga_F(VSS, NCTF)	Rev: 3A
Date: Thursday, June 15, 2006	Sheet 11 of 48	

RTC

Place near to Mini-door

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF

VCCRTC
3VPCU
D5 CH500H-40
VCCRTC_2
D4 CH500H-40
R201 1K/F
R198 1M
R195 20K/F
C457 1u/10V
G1 *SHORT_ PAD1
C452 18p/50V
C453 18p/50V
Y2 32.768KHZ
R189 10M_6
CLK_32KX1
CLK_32KX2
CN8 DFHD02MS784
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
Internal PU
C463 1u/16V_6

5VPCU
20MIL
20MIL
R197 1.2K/F
VCCRTC_1
R200 1K/F
VCCRTC_3
Q14 MMBT3904
R196 4.7K
R199 15K/F

+3VRUN
Internal PU
R148 10K
(26) SATA_LED#
SATA_LED#
Review current rating

(29) SATA_RXN0_C
(29) SATA_RXP0_C
(29) SATA_TXN0
(29) SATA_TXP0
C709 3900p/25V
C708 3900p/25V
CKL:in ~ 20nF
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
PAD T35
PAD T34
PAD T37
PAD T36
SATA_RXN2_C
SATA_RXP2_C
SATA_TXN2_C
SATA_TXP2_C

(3) CLK_PCIE_SATA#
(3) CLK_PCIE_SATA
CLK_PCIE_SATA#
CLK_PCIE_SATA

25mils/15mils
R422 24.9/F
Place within 500 mils of ICH7
SATA_BIAS

(29) PDIOR#
(29) PDIOW#
(29) PDDACK#
(29) IRQ14
(29) PIORDY
(29) PDDREQ
PDIOR#
PDIOW#
PDDACK#
IRQ14
PIORDY
PDDREQ

U36A

RTXC1
RTXC2
RTCRST#
INTRUDER#
INTVRMEN
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
ACZ_BIT_CLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIASN
SATARBIASP
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ

RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE

ICH7-M

LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#/GPIO23
LFRAME#
A20GATE
A20M#
CPUSLP#
TP1/DPRSTP#
TP2/DPSLP#
FERR#
GPIO49/CPUPWRGD
IGNNE#
INIT3_3V#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THERMTRIP#
DD0 … DD15
DA0
DA1
DA2
DCS1#
DCS3#

LAD0 (33,36,44)
LAD1 (33,36,44)
LAD2 (33,36,44)
LAD3 (33,36,44)
LDRQ#0 (36,44)
T39
LFRAME# (33,36,44)
GATEA20
GATEA20 (36)
H_A20M# (4)
R5506 close to MCH
TP_H_CPUSLP#
R104 *0
H_CPUSLP# (4,6)
H_DPRSTP# R
R121 0
H_DPSLP# R
R109 0
ICH_DPRSTP# (4,37)
H_DPSLP# (4)
H_FERR# (4)
H_PWRGD (4)
H_IGNNE# (4)
T65
H_INIT# (4)
H_INTR (4)
RCIN# (36)
H_SMI# R
R123 0
H_NMI (4)
H_SMI# (4)
H_STPCLK# (4)
H_THERMTRIP_R
PDD[15:0] (29)
PDA[2:0] (29)
PDCS1# (29)
PDCS3# (29)

+3VRUN
R404 10K
R415 10K
RCIN#
GATEA20
+1.05V
R108 *56_4
R120 *56_4
R110 56
Should be 2" close ICH7
R105 56
R103 24.9/F
PM_THRMTRIP# (4,7)
Should be 2" close ICH7
C784 *0.1u/10V

ACZ_SDIN0
ACZ_SDOUT
ACZ_SYNC
ACZ_BCLK
ACZ_RST#
R187 39
R184 39
R186 BK1005LL241-T
R174 39
ACZ_SDIN0 (30)
ACZ_SDOUT_AUDIO (30)
ACZ_SYNC_AUDIO (30)
BIT_CLK_AUDIO (30)
ACZ_RST#_AUDIO (30)
C460 *10p
C461 *10p
C459 *22p/50V
Near To ICH7-M

ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0

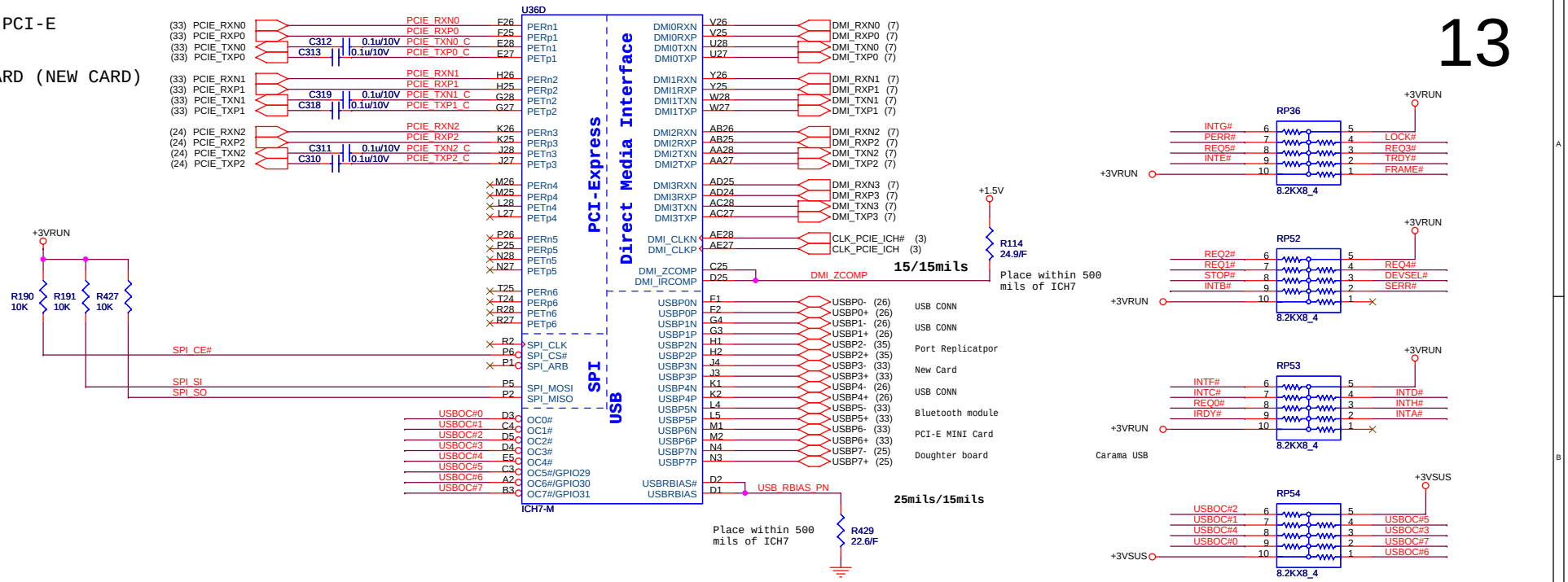
VCCRTC
R188 332K/F_6
ICH_INTVRMEN
R185 *0

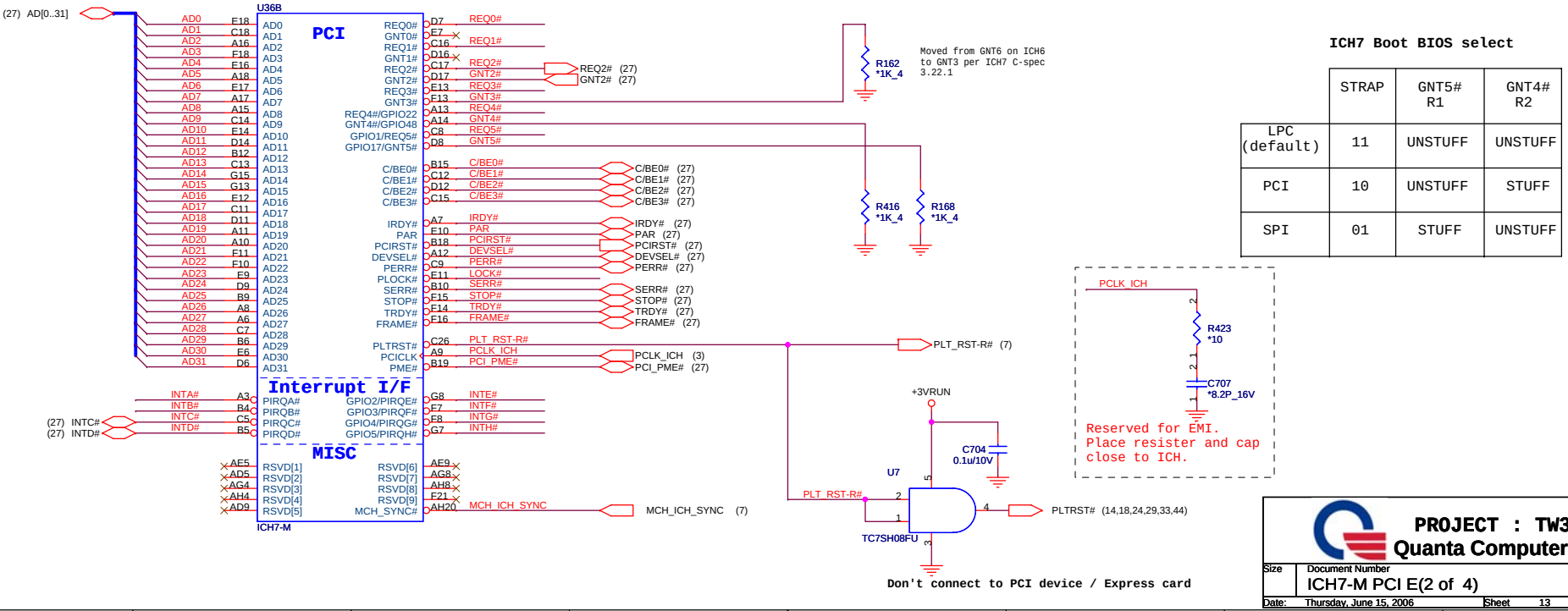
PROJECT : TW3 Quanta Computer Inc.			
Size	Document Number: ICH7-M HOST(1 of 4)		Rev 3A
Date: Thursday, June 15, 2006	Sheet 12 of 48		

MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

13





ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M PCI E(2 of 4)	3A

Date: Thursday, June 15, 2006 Sheet 13 of 48

R376

No stuff-->boot
Stuff-->No boot

+3V_S5
PCLK_SMB R124 2.2K
PDAT_SMB R128 2.2K
PCIE_WAKE# R156 680

+3V_S5
RI# R389 10K
SMB_LINK_ALERT# R391 10K
SMLINK0 R392 10K
SMLINK1 R394 10K
EXTSMI#_R R153 *10K
WAKE_SCI#_R R95 10K
SMBALERT# R395 10K

+3V_S5
SWI# R409 10K
DNBSWON# R117 10K
SYS_RST# R396 10K
PM_BATLOW# R401 8.2K/F

+3VRUN
SYS_RST# R399 *10K
CLKRUN# R420 8.2K/F
SERIRQ R412 8.2K/F
RUNTIME_SCI#_R R140 10K

SYS_RST is suspend rail

RSMRST# R424 10K

+3VRUN
R411 *1K_4
(30) ACZ_SPKR

U36C

(3,33) PCLK_SMB
(3,33) PDAT_SMB
PCLK_SMB C22
PDAT_SMB B22
SMB_LINK_ALERT# A26
SMLINK0 B25
SMLINK1 A25
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
SMB

(27) RI#
RI# A28
RI#

A19
SPKR
(27,44) SUS_STAT#
(4) SYS_RST#
SUS_STAT# A27
SYS_RST# A22
SPKR
SUS_STAT#
SYS_RST#

(7) PM_BMBUSY#
R166 0
AB18
GPIO0/BM_BUSY#

T24
SMBALERT# B23
GPIO11/SMBALERT#

+3VRUN
R126 *10K
R129 *10K
No ASF support
(3) PM_STPPCI#
(3) PM_STPCPU#
R130 0
R127 0
PM_STPPCI_ICH# AC20
PM_STPCPU_ICH# AF21
GPIO18/STPPCI#
GPIO20/STPCPU#

T64
A21
GPIO26

T66
T22
B21
F23
GPIO27
GPIO28

+3VRUN
R418 8.2K/F
(27,36,44) CLKRUN#
CLKRUN# AG18
GPIO32/CLKRUN#

(29) ICH_GPO33
ICH_GPO33 AC19
BOARD_ID2 U2
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#

(24,33) PCIE_WAKE#
(27,36,44) SERIRQ
PCIE_WAKE# F20
SERIRQ AH21
AE20
WAKE#
SERIRQ
THRM#

(5) THERM_ALERT#

VR_PWRGD_CK410 AD22
VRMPWRGD

T28
R141 0
R143 0
(36) SCI#
(36) KBSMI#
RUNTIME_SCI#_R AC21
EXTSMI#_R AC18
F21
GPIO6
GPIO7
GPIO8

ICH7-M

SYS GPIO Power MGT

SATA GPIO
Clocks

GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
AE19 BOARD_ID1
AH18 BOARD_ID0
AH19 BOARD_ID3
AE19 BOARD_ID4

CLK14 AC1 14M_ICH
CLK48 B2 CLKUSB_48
14M_ICH (3)
CLKUSB_48 (3)

SUSCLK C20 ICH_SUSCLK
T31

SLP_S3# B24 R115 100/F
SLP_S4# D23 R122 100/F
SLP_S5# F22
SUSB# (36)
SUSC# (36)
T21

PWROK AA4 ICH_PWROK

GPIO16/DPRSLPVR AC22 PM_DPRSLPVR_R R113 100/F
R116 0
R112 *100K
PM_EXTTS#1 (7)
PM_DPRSLPVR (37)
CKL :100Kohm PD

TP0/BATLOW# C21 PM_BATLOW#_R R400 100/F
PM_BATLOW# (36)

PWRBTN# C23 DNBSWON#
R158 100K
DNBSWON# (36)

LAN_RST# C19
R98 0
PLTRST# (13,18,24,29,33,44)

RSMRST# Y4 PM_RSMRST#_R R425 100/F RSMRST#
RSMRST# (36)

GPIO9 E20 SWI#
GPIO10 A20
GPIO12 E19 WAKE_SCI#_R
GPIO13 R4
GPIO14 E22
GPIO15 R3
GPIO24 D20
GPIO25 AD21
GPIO35 AD20 GPIO38
GPIO38 AE20
GPIO39

SWI# (36)
T67
T27
T19
T40
T25
T29
T30

GPIO

+3VRUN
U14
(3,37) CLK_EN#
VR_PWRGD_CK410
NL17SZ14DFT2G

Note: External pull-up 3V

GPIO25 /Suspend rail is a HW strap , don't pull down .

PWM require 6.9K
Change to 6.8K
+3VSUS
C451 0.047u/10V
+3VRUN
R193 6.8K
(7,37) DELAY_VR_PWRGOOD
(36) PWROK
U15
TC7SH08FU
ICH_PWROK
R182 100K
R183 10K

Level is incorrect !!

Place these close to ICH7.
CLKUSB_48
R428 *10
C712 *4.7P_50V
14M_ICH
R372 *10_NC
C637 *4.7P_50V_NC

+3VRUN
R421 *10K_4
BOARD_ID0
R167 10K

+3VRUN
R147 *10K
BOARD_ID1
R139 10K

+3VRUN
R371 *10K_NC
BOARD_ID2
R367 10K

+3VRUN
R136 *10K
BOARD_ID3
R137 10K

+3VRUN
R368 10K
BOARD_ID4
R366 *10K

+3VRUN
R482 10K
GPIO38
R483 *10K

GPIO38	Function
High	CRT
Low	DVI

Board ID	Function
ID [1:0]	00: TW3 01: DW1
ID2	0: SATA HDD 1: PATA HDD
ID3	Reserve
ID4	0: No docking. 1: w/ docking

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M GPIO(3 of 4)	3B

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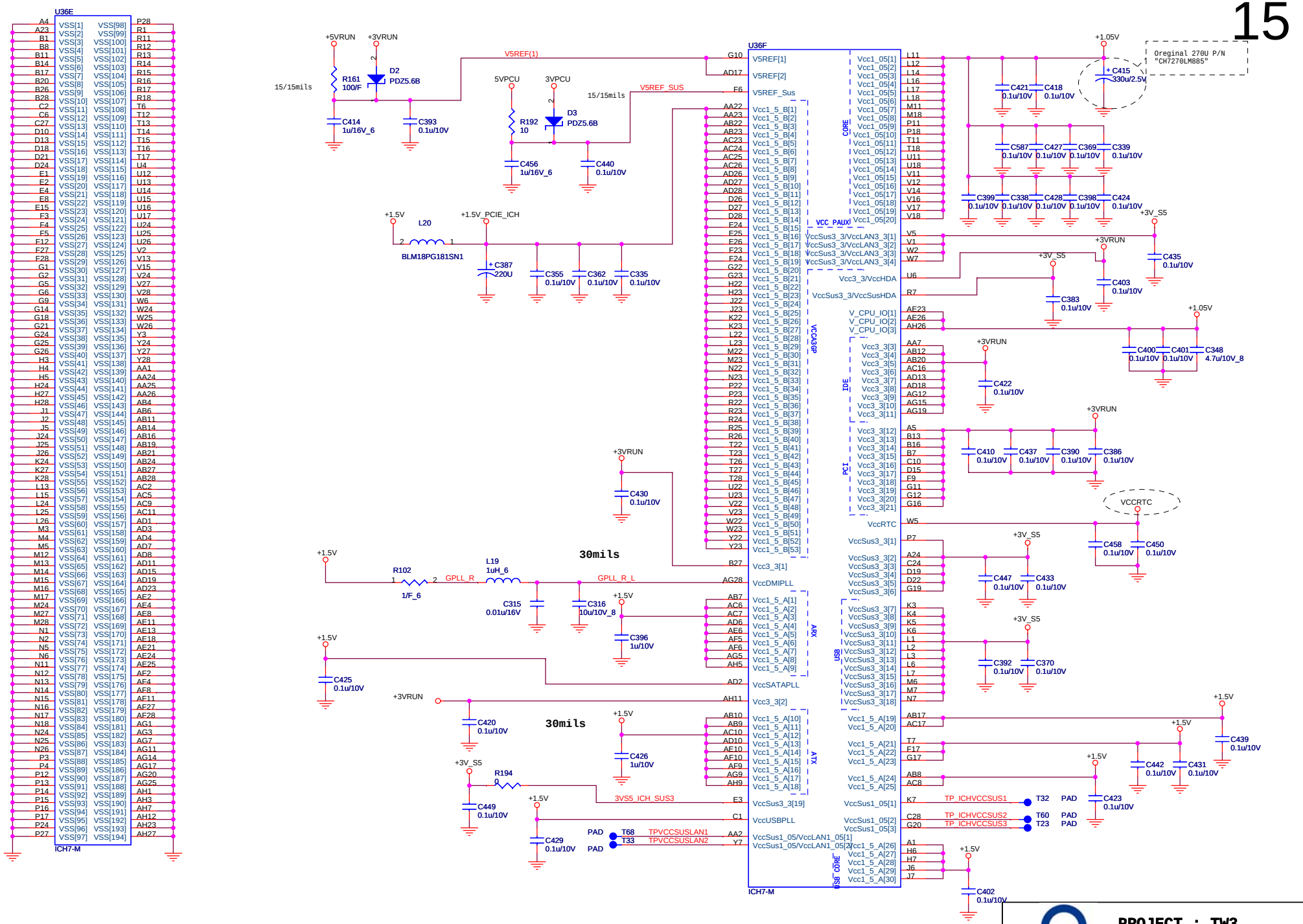

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M POWER(4 of 4)	3A

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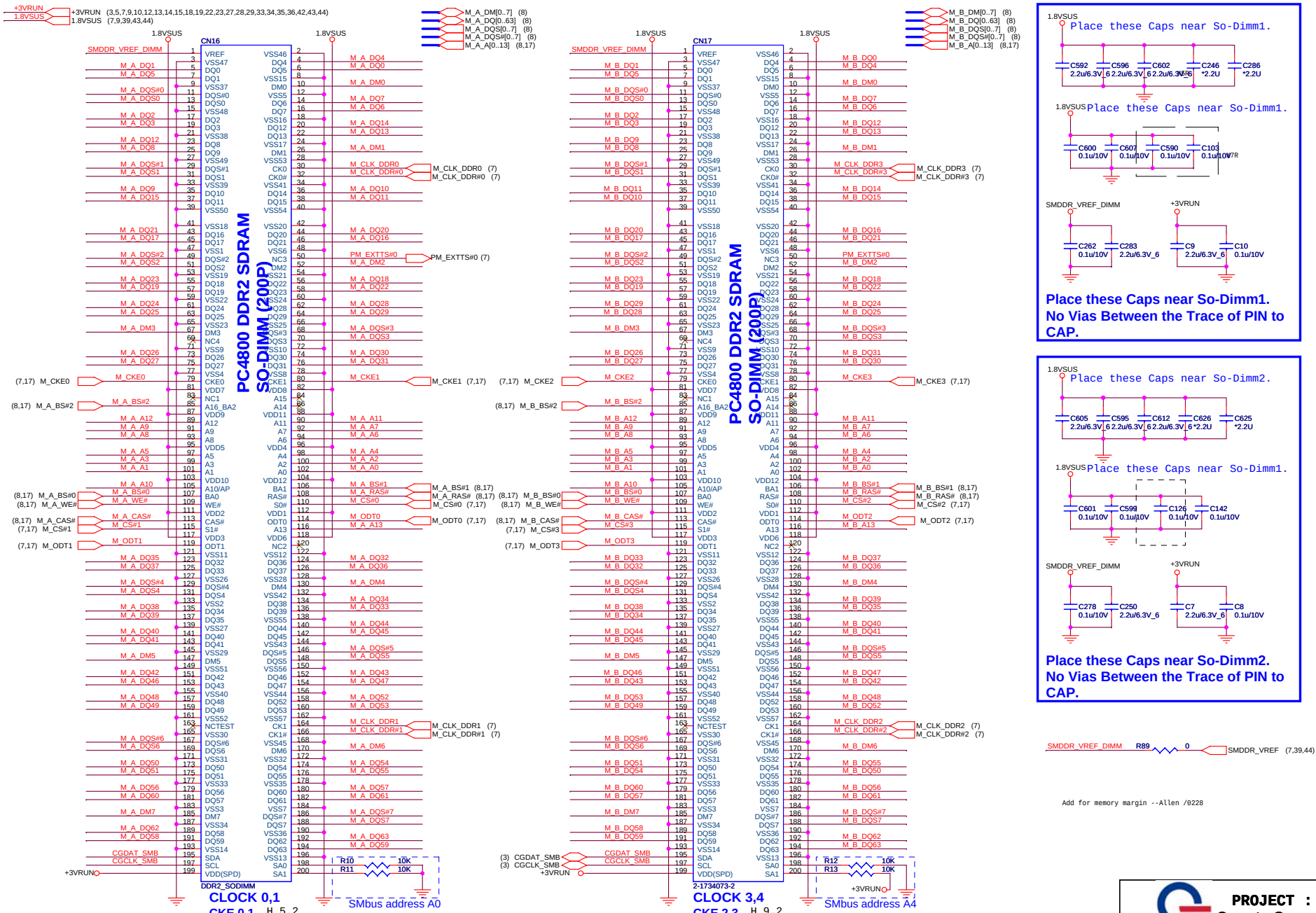

Add for memory margin --Allen /0228

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	DDRII SO-DIMM(200P)	3A

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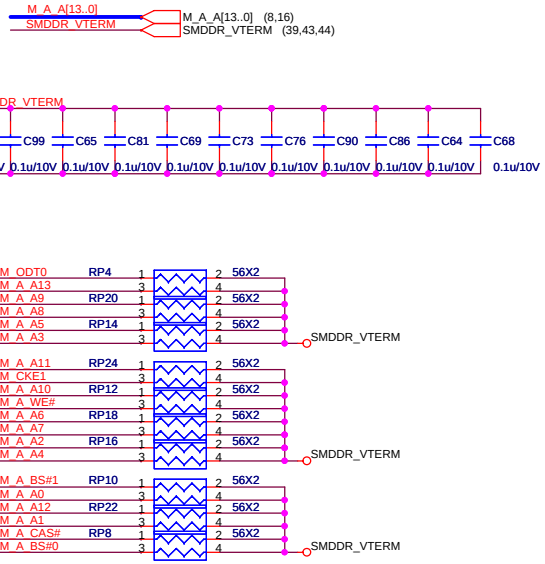
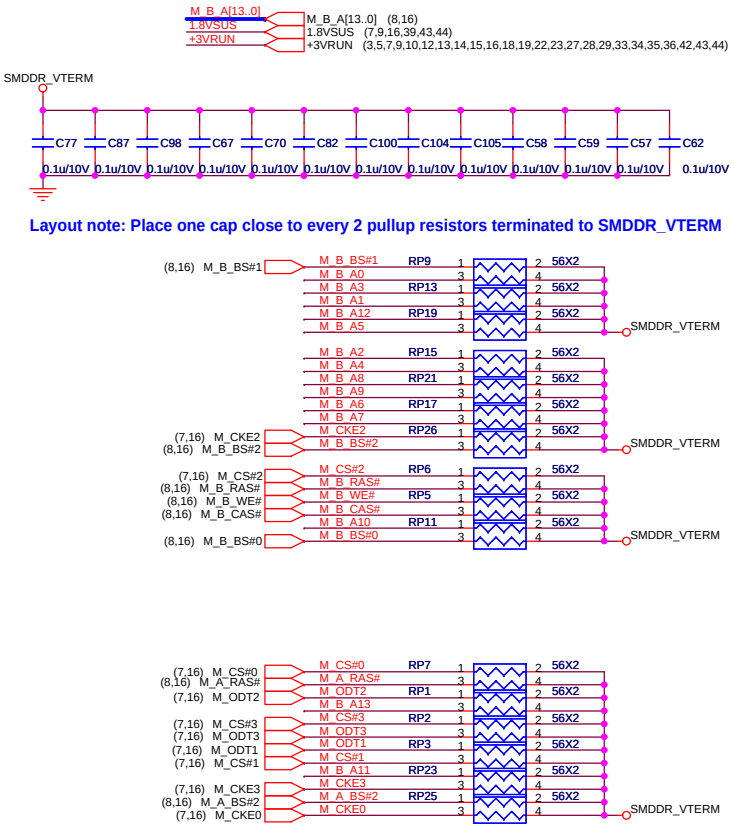
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL



DDRII B CHANNEL



PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number	Rev
	DDRII TERMINATION	3A
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(7) PEG_RXP[15:0]
(7) PEG_RXN[15:0]
(7) PEG_TXP[15:0]
(7) PEG_TXN[15:0]

U31A
PART 1 OF 4
PCI-EXPRESS INTERFACE
Clock
PCIE Power
G72M

PEG_TXP0 AF1 PEX_RX0P
PEG_TXN0 AG2 PEX_RX0N
PEG_TXP1 AG3 PEX_RX1P
PEG_TXN1 AG4 PEX_RX1N
PEG_TXP2 AE4 PEX_RX2P
PEG_TXN2 AF5 PEX_RX2N
PEG_TXP3 AG6 PEX_RX3P
PEG_TXN3 AG7 PEX_RX3N
PEG_TXP4 AF7 PEX_RX4P
PEG_TXN4 AF8 PEX_RX4N
PEG_TXP5 AG9 PEX_RX5P
PEG_TXN5 AG10 PEX_RX5N
PEG_TXP6 AE10 PEX_RX6P
PEG_TXN6 AF11 PEX_RX6N
PEG_TXP7 AG12 PEX_RX7P
PEG_TXN7 AG13 PEX_RX7N
PEG_TXP8 AG15 PEX_RX8P
PEG_TXN8 AG16 PEX_RX8N
PEG_TXP9 AF16 PEX_RX9P
PEG_TXN9 AF17 PEX_RX9N
PEG_TXP10 AG18 PEX_RX10P
PEG_TXN10 AG19 PEX_RX10N
PEG_TXP11 AF19 PEX_RX11P
PEG_TXN11 AF20 PEX_RX11N
PEG_TXP12 AG21 PEX_RX12P
PEG_TXN12 AG22 PEX_RX12N
PEG_TXP13 AF22 PEX_RX13P
PEG_TXN13 AF23 PEX_RX13N
PEG_TXP14 AG24 PEX_RX14P
PEG_TXN14 AG25 PEX_RX14N
PEG_TXP15 AG26 PEX_RX15P
PEG_TXN15 AF27 PEX_RX15N

(3) CLK_PCIE_VGA AE3 PEX_REFCLK
(3) CLK_PCIE_VGA# AE4 PEX_REFCLK#

PEX_TX0P AD5 V_GMCHEXP_RXP0
PEX_TX0N AD6 V_GMCHEXP_RXN0
PEX_TX1P AE6 V_GMCHEXP_RXP1
PEX_TX1N AE7 V_GMCHEXP_RXN1
PEX_TX2P AD7 V_GMCHEXP_RXP2
PEX_TX2N AC7 V_GMCHEXP_RXN2
PEX_TX3P AE9 V_GMCHEXP_RXP3
PEX_TX3N AE10 V_GMCHEXP_RXN3
PEX_TX4P AD10 V_GMCHEXP_RXP4
PEX_TX4N AC10 V_GMCHEXP_RXN4
PEX_TX5P AE12 V_GMCHEXP_RXP5
PEX_TX5N AE13 V_GMCHEXP_RXN5
PEX_TX6P AD13 V_GMCHEXP_RXP6
PEX_TX6N AC13 V_GMCHEXP_RXN6
PEX_TX7P AC15 V_GMCHEXP_RXP7
PEX_TX7N AD15 V_GMCHEXP_RXN7
PEX_TX8P AE15 V_GMCHEXP_RXP8
PEX_TX8N AE16 V_GMCHEXP_RXN8
PEX_TX9P AC18 V_GMCHEXP_RXP9
PEX_TX9N AD18 V_GMCHEXP_RXN9
PEX_TX10P AE18 V_GMCHEXP_RXP10
PEX_TX10N AE19 V_GMCHEXP_RXN10
PEX_TX11P AC21 V_GMCHEXP_RXP11
PEX_TX11N AD21 V_GMCHEXP_RXN11
PEX_TX12P AE21 V_GMCHEXP_RXP12
PEX_TX12N AE22 V_GMCHEXP_RXN12
PEX_TX13P AD22 V_GMCHEXP_RXP13
PEX_TX13N AD23 V_GMCHEXP_RXN13
PEX_TX14P AE25 V_GMCHEXP_RXP14
PEX_TX14N AE25 V_GMCHEXP_RXN14
PEX_TX15P AE24 V_GMCHEXP_RXP15
PEX_TX15N AD24 V_GMCHEXP_RXN15

PEX_TSTCLK_OUT AF13 PEX_TSTCLK
PEX_TSTCLK_OUT# AF14 PEX_TSTCLK#
PEX_RST# AC6

R93 *200/F
R386 0

U33 *TC7SH08FU
+3VRUN
C651 *0.1u/10V
PLTRST# (13,14,24,29,33,44)

PEX_IOVDD_01 AB10
PEX_IOVDD_02 AB11
PEX_IOVDD_03 AB14
PEX_IOVDD_04 AB15
PEX_IOVDD_05 W17
PEX_IOVDD_06 W18
PEX_IOVDD_07 AB20
PEX_IOVDD_08 AB21

PEX_IOVDDQ_01 AA4
PEX_IOVDDQ_02 AB5
PEX_IOVDDQ_03 AB6
PEX_IOVDDQ_04 AB7
PEX_IOVDDQ_05 AB8
PEX_IOVDDQ_06 AB9
PEX_IOVDDQ_07 AC9
PEX_IOVDDQ_08 AC11
PEX_IOVDDQ_09 AB12
PEX_IOVDDQ_10 AC12
PEX_IOVDDQ_11 AB13
PEX_IOVDDQ_12 AB16
PEX_IOVDDQ_13 AC16
PEX_IOVDDQ_14 AB17
PEX_IOVDDQ_15 AC17
PEX_IOVDDQ_16 AB18
PEX_IOVDDQ_17 AB19
PEX_IOVDDQ_18 AC19
PEX_IOVDDQ_19 AC20

VDD_LP_01 W9
VDD_LP_02 W10
VDD_LP_03 W11
VDD_LP_04 W12

VDD33_01 J12
VDD33_02 F13
VDD33_03 J13
VDD33_04 F14
VDD33_05 J15
VDD33_06 J16

NC_01 D12
NC_02 E12
NC_03 F12
NC_04 C13

VDD_01 J9
VDD_02 M9
VDD_03 N9
VDD_04 R9
VDD_05 T9
VDD_06 J10
VDD_07 J11
VDD_08 M11
VDD_09 N11
VDD_10 R11
VDD_11 T11
VDD_12 L12
VDD_13 M12
VDD_14 T12
VDD_15 U12
VDD_16 L13
VDD_17 M13
VDD_18 T13
VDD_19 U13
VDD_20 W13
VDD_21 M14
VDD_22 T14
VDD_23 L15
VDD_24 M15
VDD_25 T15
VDD_26 U15
VDD_27 W15
VDD_28 L16
VDD_29 M16
VDD_30 T16
VDD_31 U16
VDD_32 W16
VDD_33 M17
VDD_34 N17
VDD_35 R17
VDD_36 T17

PEX_PLLVDD Y6
PEX_PLLDVDD AA5
PEX_PLLGND AA6

C304 0.1u/10V PEG_RXP0 V_GMCHEXP_RXP0
C656 0.1u/10V PEG_RXP1 V_GMCHEXP_RXP1
C314 0.1u/10V PEG_RXP2 V_GMCHEXP_RXP2
C664 0.1u/10V PEG_RXP3 V_GMCHEXP_RXP3
C326 0.1u/10V PEG_RXP4 V_GMCHEXP_RXP4
C684 0.1u/10V PEG_RXP5 V_GMCHEXP_RXP5
C368 0.1u/10V PEG_RXP6 V_GMCHEXP_RXP6
C688 0.1u/10V PEG_RXP7 V_GMCHEXP_RXP7
C385 0.1u/10V PEG_RXP8 V_GMCHEXP_RXP8
C690 0.1u/10V PEG_RXP9 V_GMCHEXP_RXP9
C353 0.1u/10V PEG_RXP10 V_GMCHEXP_RXP10
C693 0.1u/10V PEG_RXP11 V_GMCHEXP_RXP11
C361 0.1u/10V PEG_RXP12 V_GMCHEXP_RXP12
C696 0.1u/10V PEG_RXP13 V_GMCHEXP_RXP13
C364 0.1u/10V PEG_RXP14 V_GMCHEXP_RXP14
C699 0.1u/10V PEG_RXP15 V_GMCHEXP_RXP15

C309 0.1u/10V PEG_RXN0 V_GMCHEXP_RXN0
C657 0.1u/10V PEG_RXN1 V_GMCHEXP_RXN1
C323 0.1u/10V PEG_RXN2 V_GMCHEXP_RXN2
C663 0.1u/10V PEG_RXN3 V_GMCHEXP_RXN3
C332 0.1u/10V PEG_RXN4 V_GMCHEXP_RXN4
C685 0.1u/10V PEG_RXN5 V_GMCHEXP_RXN5
C367 0.1u/10V PEG_RXN6 V_GMCHEXP_RXN6
C687 0.1u/10V PEG_RXN7 V_GMCHEXP_RXN7
C384 0.1u/10V PEG_RXN8 V_GMCHEXP_RXN8
C689 0.1u/10V PEG_RXN9 V_GMCHEXP_RXN9
C352 0.1u/10V PEG_RXN10 V_GMCHEXP_RXN10
C692 0.1u/10V PEG_RXN11 V_GMCHEXP_RXN11
C360 0.1u/10V PEG_RXN12 V_GMCHEXP_RXN12
C695 0.1u/10V PEG_RXN13 V_GMCHEXP_RXN13
C363 0.1u/10V PEG_RXN14 V_GMCHEXP_RXN14
C698 0.1u/10V PEG_RXN15 V_GMCHEXP_RXN15

+1.2V_GFX_PCIE
L14 BLM11A121S
G72_PLLAVDD
C242 4.7u/6.3V_6
C192 0.1u/10V

+VCC_GFX_CORE
C247 100p/50V
C189 0.01u/16V
C197 0.01u/16V
C168 100p/50V
C181 0.01u/16V
C228 220p/50V
C240 100p/50V
C223 220p/50V
C205 100p/50V
C170 1u/10V
C224 220p/50V
C185 0.01u/16V
C238 220p/50V
C225 220p/50V
C219 10u/6.3V_6
C245 10u/6.3V_6
C188 10u/6.3V_6

+1.2V_GFX_PCIE
L17 BLM11A121S
PEX_PLL_AVDD
PEX_PLL_DVDD
C285 4.7u/6.3V_6
C281 1u/10V
C280 1u/10V
C241 0.1u/10V
C255 0.01u/16V

+1.2V_GFX_PCIE
C266 0.022u/16V
C274 0.022u/16V
C273 0.022u/16V
C258 10u/6.3V_6
C261 1u/10V
C277 4.7u/6.3V_6
PLACE NEAR BALLS
PLACE NEAR GPU

+1.2V_GFX_PCIE
C259 10u/6.3V_6
C271 0.022u/16V
C276 0.1u/10V
C272 0.1u/10V
C260 1u/10V
C606 4.7u/6.3V_6
PLACE NEAR BALLS

+VCC_GFX_CORE
C209 220p/50V
C193 0.01u/16V
C249 0.1u/10V

+3VRUN
C169 0.1u/10V
C173 4700p/25V
C230 0.022u/16V
C155 1u/10V
PLACE NEAR BALLS

PROJECT : TW3
Quanta Computer Inc.

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	NV72M-1	3A

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U31B — PART 2 OF 4 — VIDEO & MULTIMEDIA (Multi-Use Input/Output Interface)

Integrated TMDS

RAM_CFG[3:0]	RAM_CFG[3:0]	Vendor
0000	DDR2 16Mx16x4,64bit,128MB	Elpida
0001	DDR2 16Mx16x4,64bit,128MB	Samsung
0010	DDR2 16Mx16x4,64bit,128MB	Infineon
0011	DDR2 16Mx16x4,64bit,128MB	Hynix
0100	Reserve	
0101	DDR2 32Mx16x4,64bit,256MB	Samsung
0110	DDR2 32Mx16x4,64bit,256MB	Infineon
0111	DDR2 32Mx16x4,64bit,256MB	Hynix
1000	DDR2 16Mx16x2,32bit,64MB	Elpida
1001	DDR2 16Mx16x2,32bit,64MB	Samsung
1010	DDR2 16Mx16x2,32bit,64MB	Infineon
1011	DDR2 16Mx16x2,32bit,64MB	Hynix

PCI_DEVID[3:0]	Description
0111	G72MV
1000	G72M

G72MV: AJ073000T06 IC (820P) GF-GO7300-B-N-A3 (BGA) EU

64M: AKD5JG-TW12 HYNIX HY5PS561621AFP-25

128M: AKD5JG-T^08 INFINEON HYB18T256161AFL25

Ground guard trace required for VGATHRM+/- trace

15 MIL

10 mil trace / 10 mil space

Layout footprint : MSOP8

SLAVE ADDRESS: 9C

Place close to VGA Chip

PROJECT	TW3
Quanta Computer Inc.	
Size	B
Document Number	NV72M-2
Rev	3B
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FB_CMD[0..26] (21)
FBD[0..63] (21)
FBDQM[0..7] (21)
FBDQS[0..7] (21)
FBDQS#[0..7] (21)

U31C
Part 3 of 4
MEMORY INTERFACE
G72M

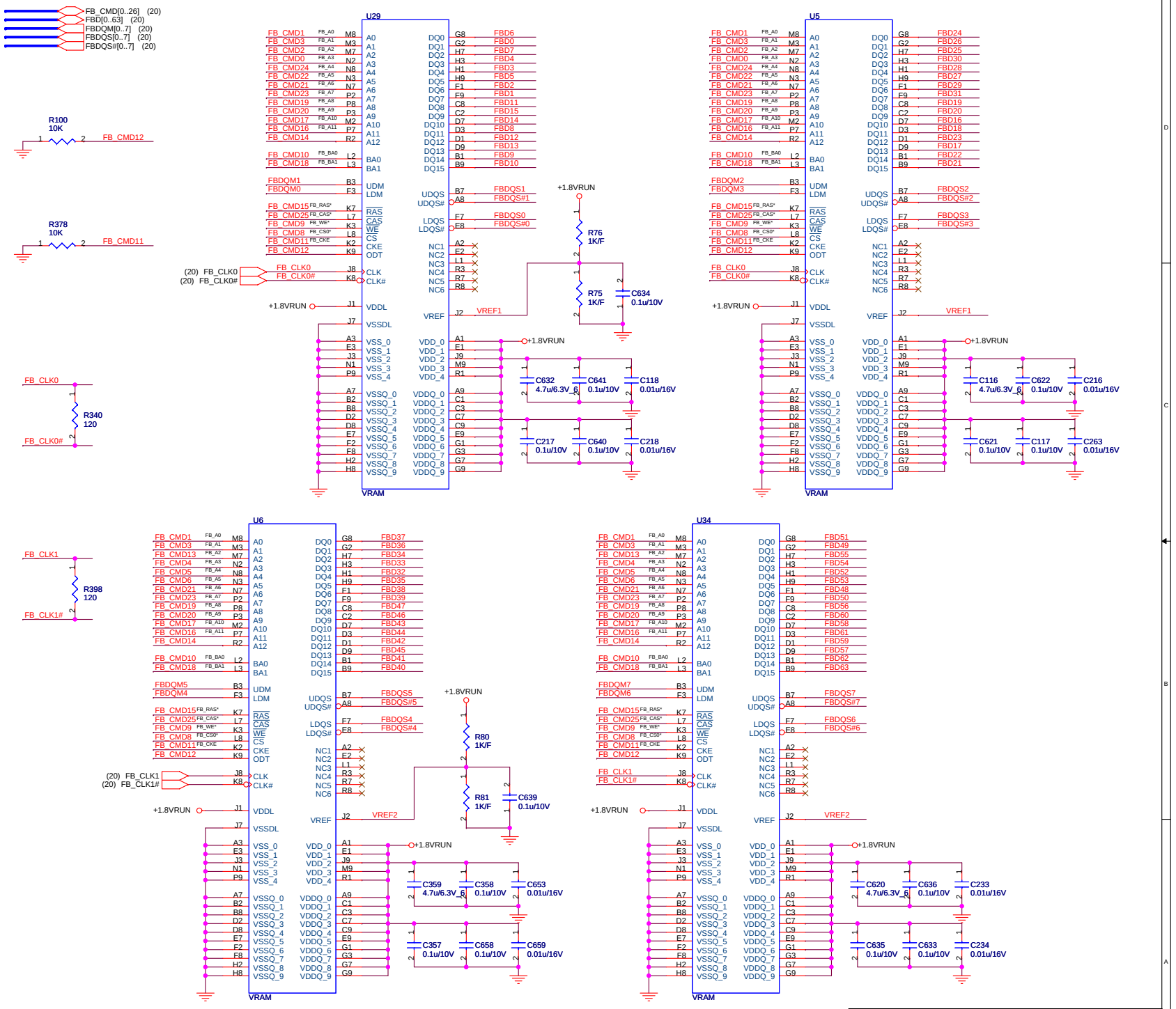
U31D
Part 4 of 4
GND
G72M

FBVREF = FBVDDQ * Rb/(Rt + Rb).
VREF = 0.5 * FBVDDQ.
DDR: 0.9V = 1.8V * 1K/(1K + 1K).

PLACE BELOW GPU

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	NV72M-3	3A
Date: Thursday, June 15, 2006	Sheet 20 of 48	



PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	NV72M-4	3A
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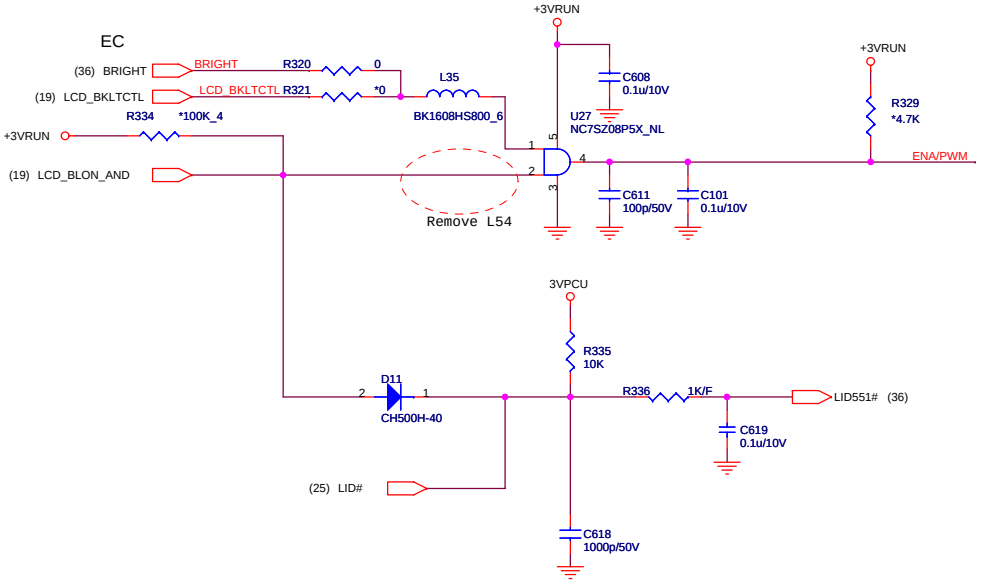
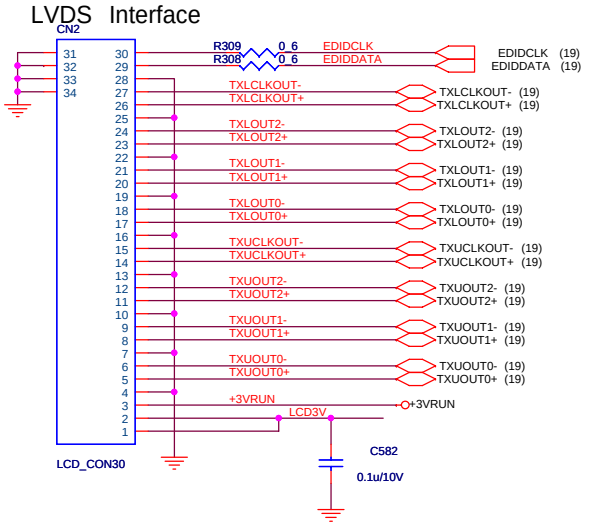
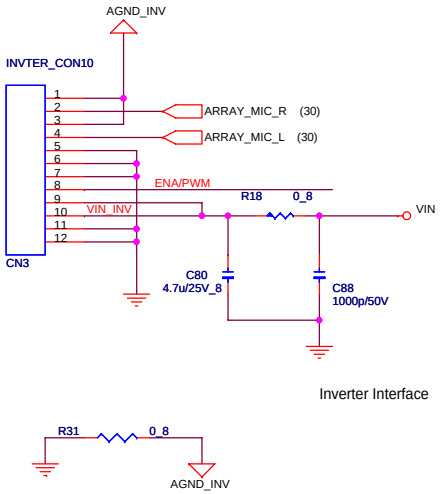
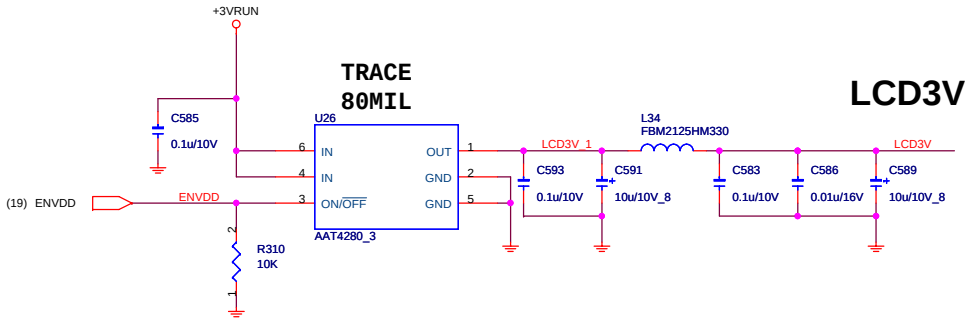






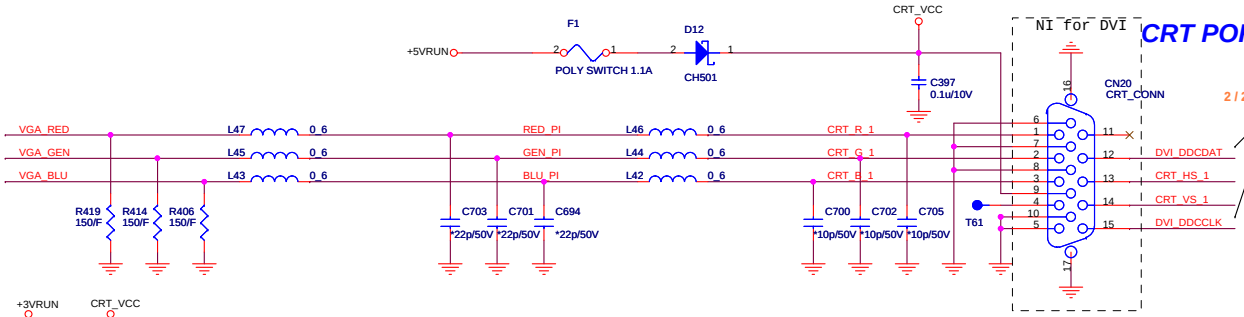
Inverter Interface



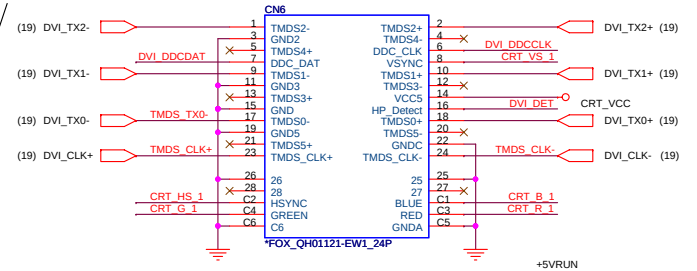
PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	LCD,INVERTER CONN	3A
Date: Thursday, June 15, 2006	Sheet 22 of 48	

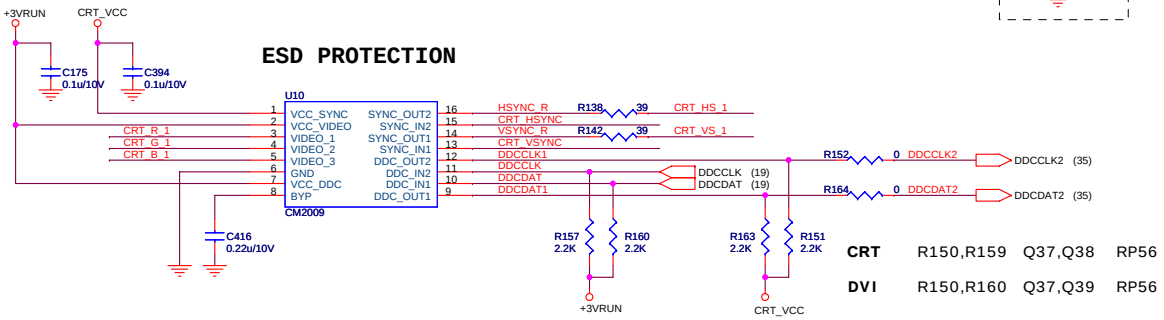
CRT PORT



2/22 Tony Huang



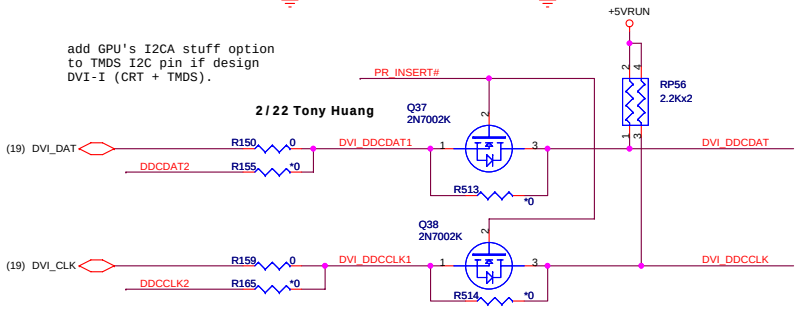
ESD PROTECTION



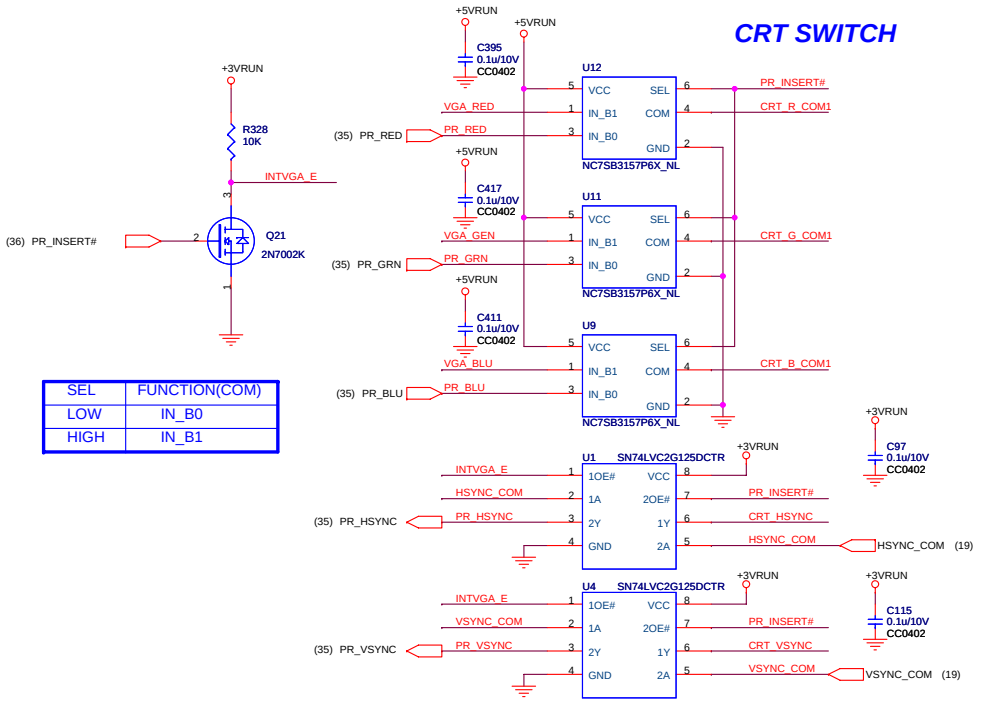
CRT	R150,R159	Q37,Q38	RP56
DVI	R150,R160	Q37,Q39	RP56

add GPU's I2CA stuff option
to TMDS I2C pin if design
DVI-I (CRT + TMDS).

2/22 Tony Huang



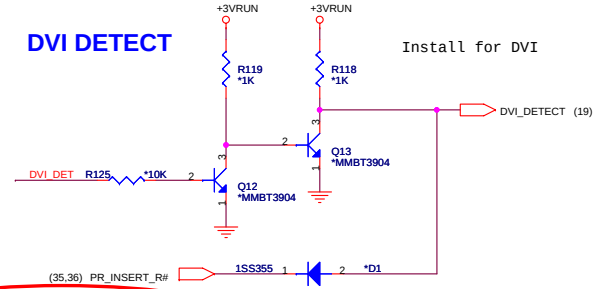
CRT SWITCH

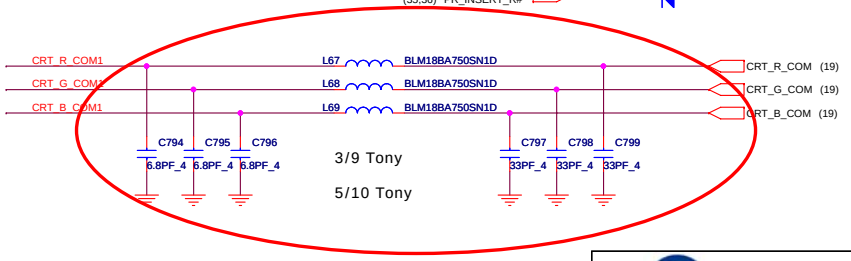


SEL	FUNCTION(COM)
LOW	IN_B0
HIGH	IN_B1

DVI DETECT

Install for DVI





PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	CRT,TV-OUT,DVI CONN.	3B

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C: 88E8053 LF PN: AJ080530010 (20050414)

1Mbits

C: Add 9 X GND Pad for LAN controller. (20050411)

C: Add these GND pin for via hole to GND Plane.

C: Add RC (R37 change to 200K, Add C101) delay to control LOM_DISABLE#. (20050411)

C: Reserve R36. Change LANRST# to PCIRST# source from MB option modify.(2005/04/11)

CLOSE CHIP

DELAY PIN10 AT LEAST 150ms

88E8038/88E8055

FOR 8038	
R389	2K
R9	NC

LANVCC

PLACEMENT CLOSE TO EACH OTHER

C: Widen to 20 mils. AVDD25 to 20 mils.(20050411)

C: Widen to 20 mils. VDD to 20 mils.(20050411)

0804 REDUCING THE LANVCC NOISE

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Marvell 88E8036,88E8053	3A

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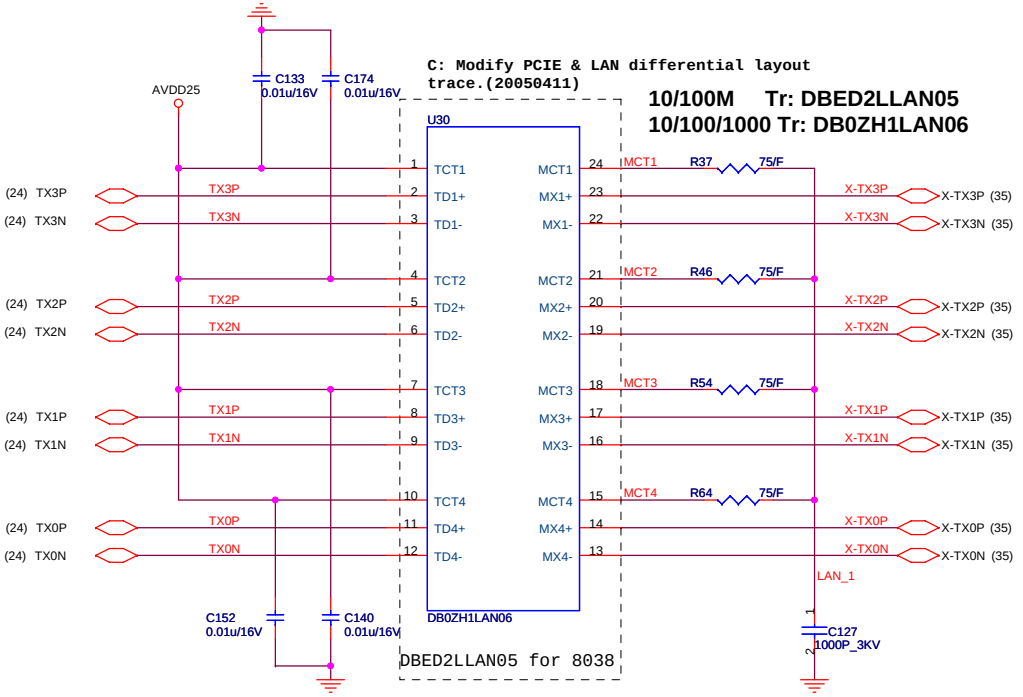

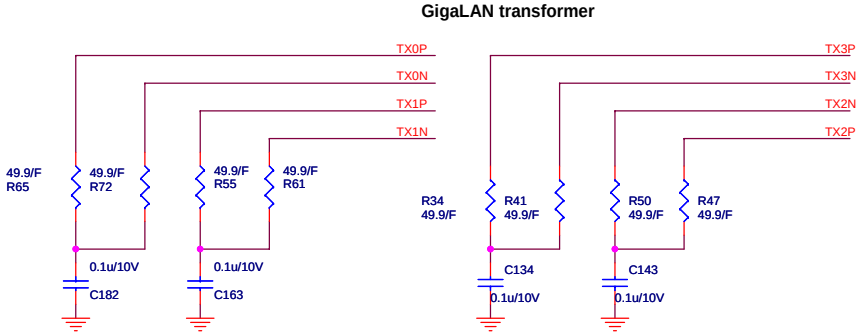

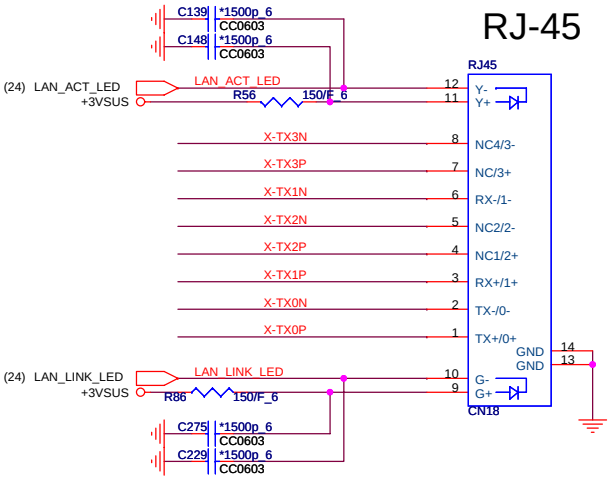

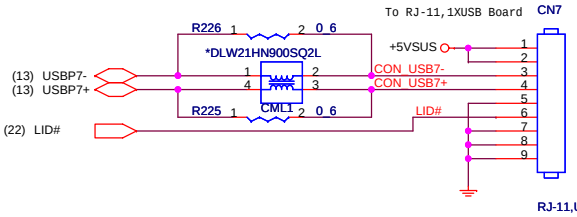

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	LAN SW CONN& MDC CONN	3A

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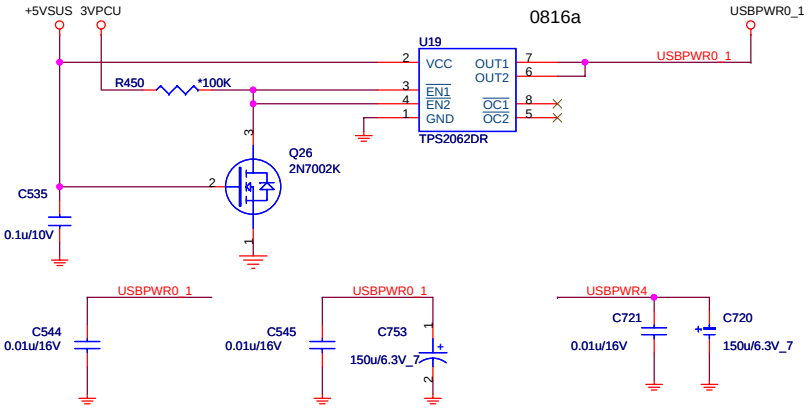
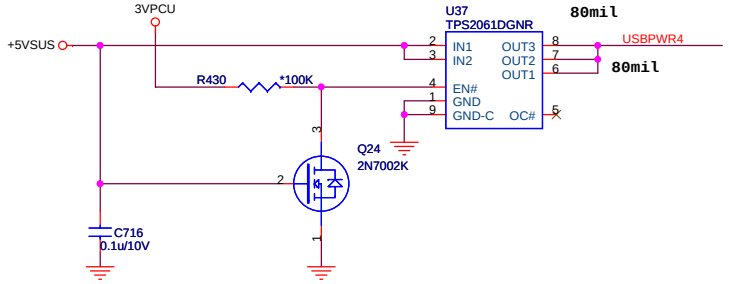
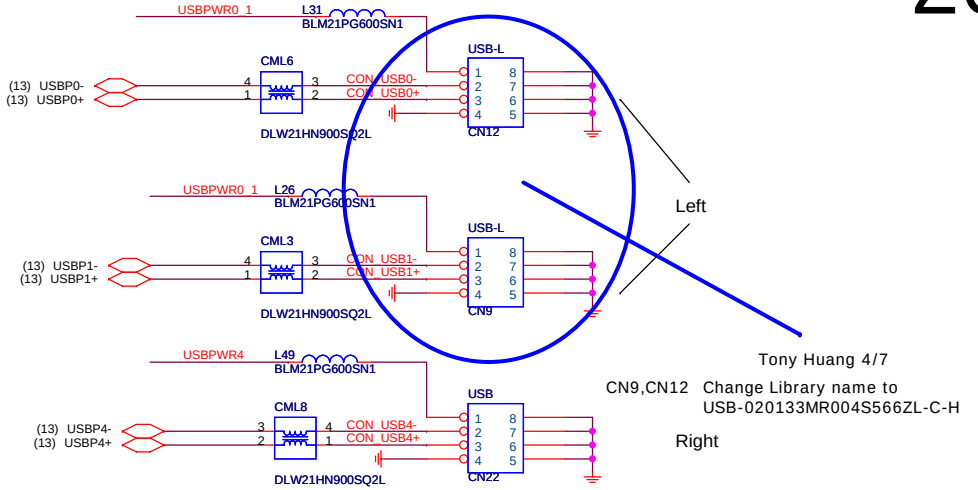


C:Change U1 from G528 to TPS2061



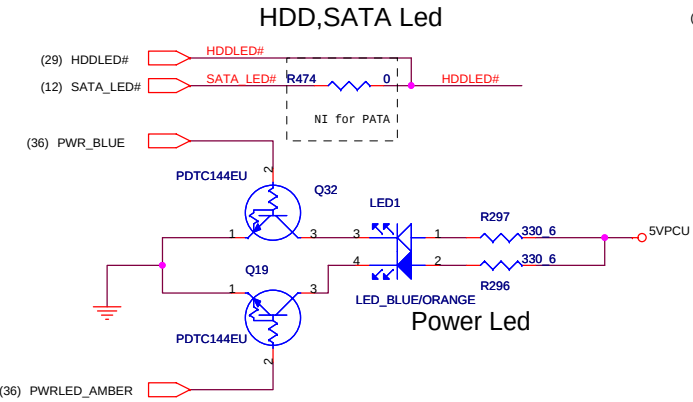
USB Port

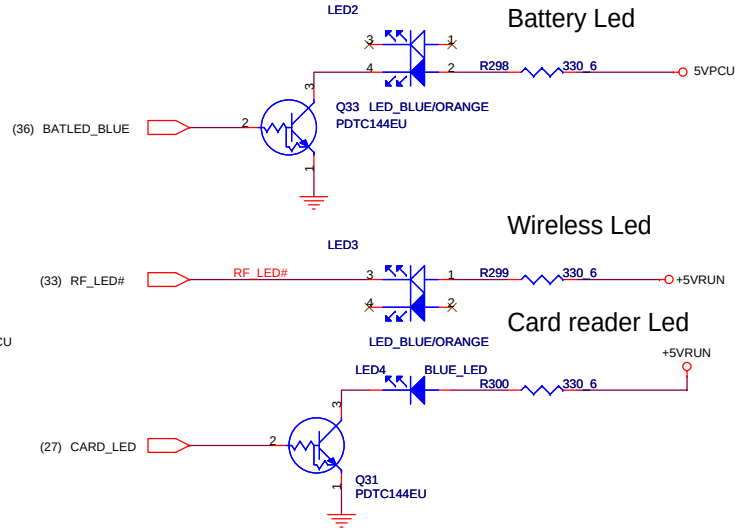


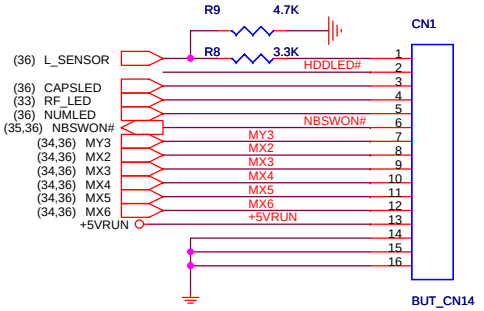
Tony Huang 4/7

CN9,CN12 Change Library name to USB-020133MR004S566ZL-C-H

For Botton Board







PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	USB,LED,Buttom/B	3B
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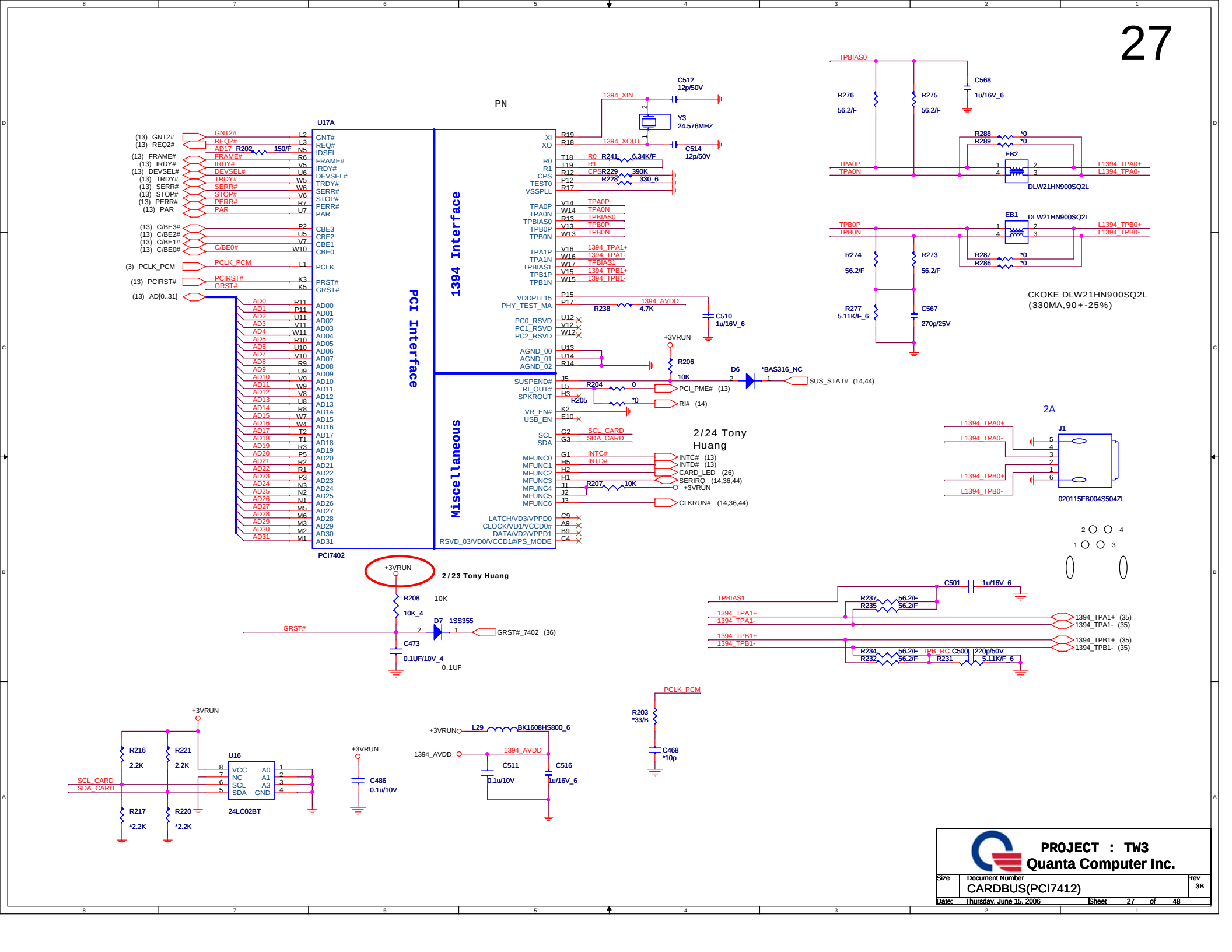

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Quanta Computer Inc.			
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	CARDBUS(PCI7412)		3B
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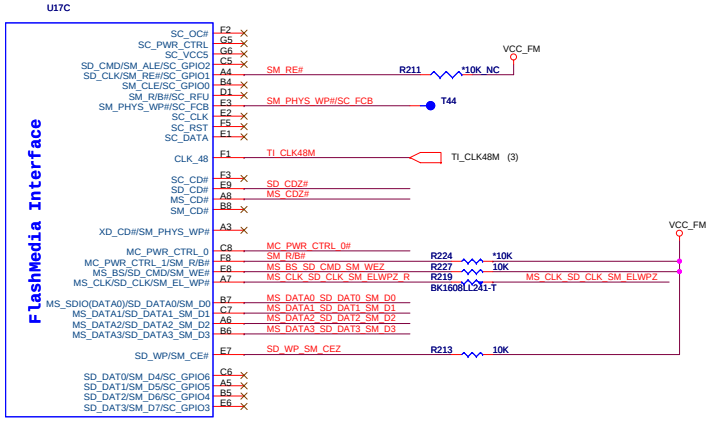
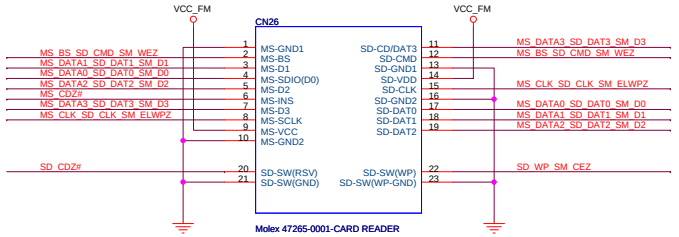
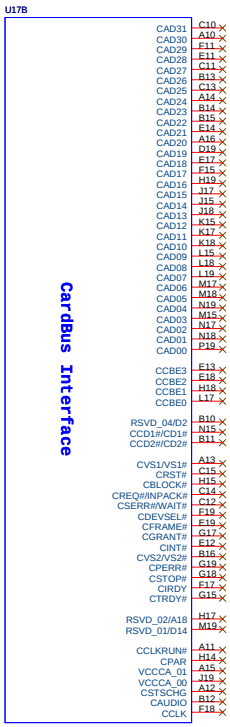
DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

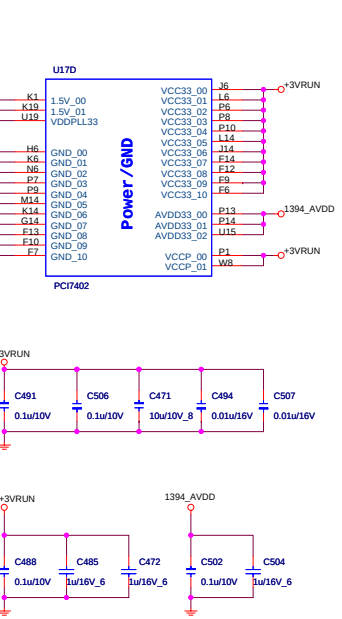
3 IN1 CARD READER (push-push)

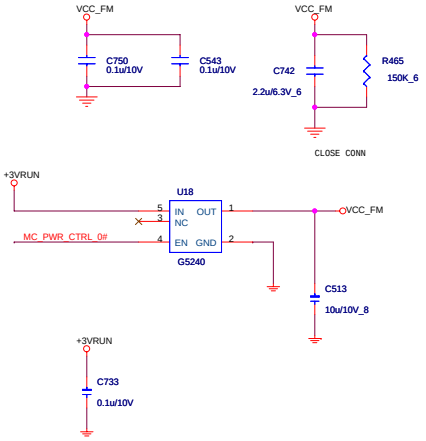




Supporting MMC/SD/MS Cards
Molex P/N:DFHD23MS0B6







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	1394 CONTROLLER	3A

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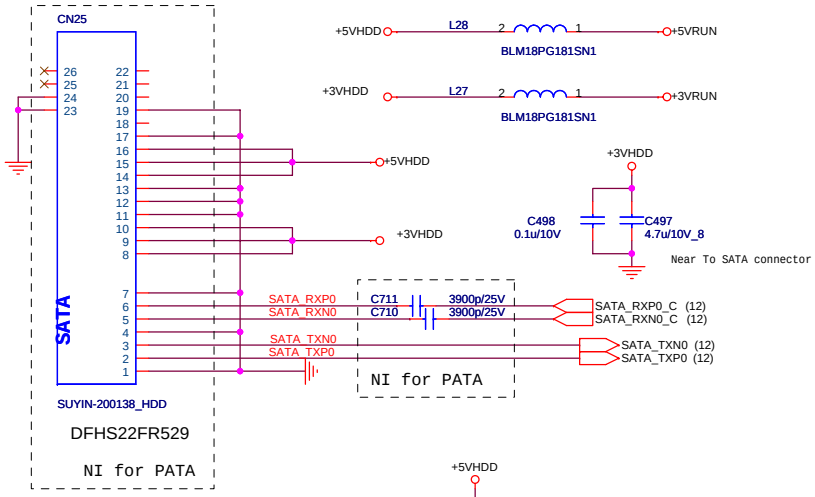
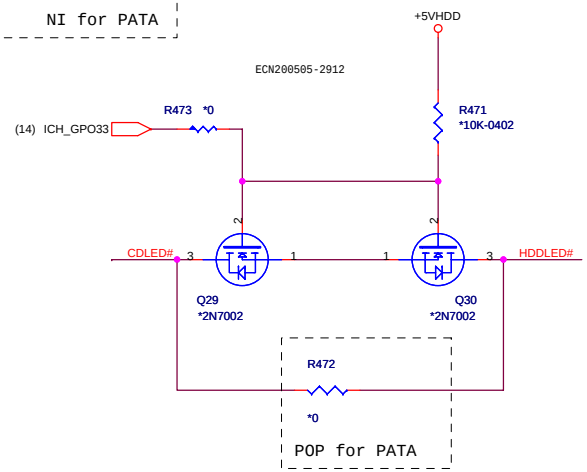
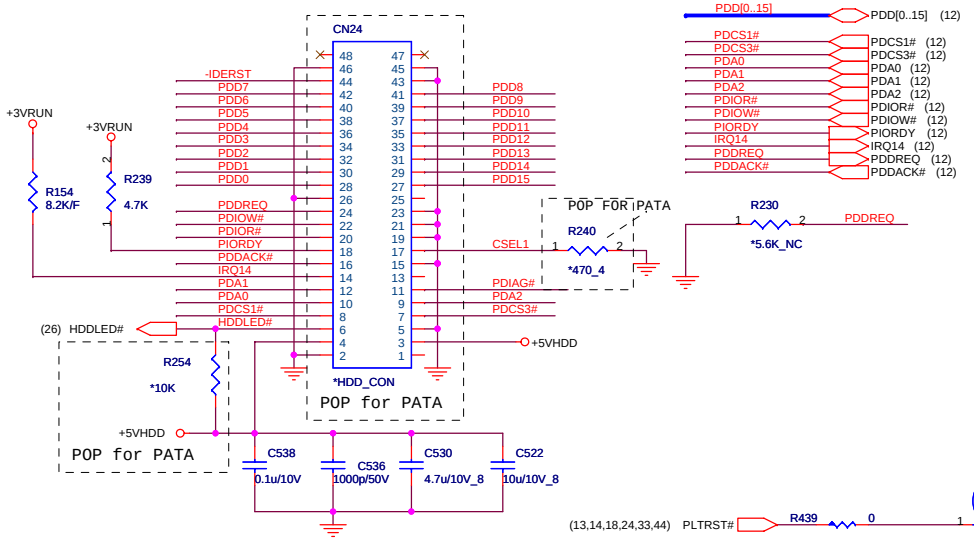
SATA HDD

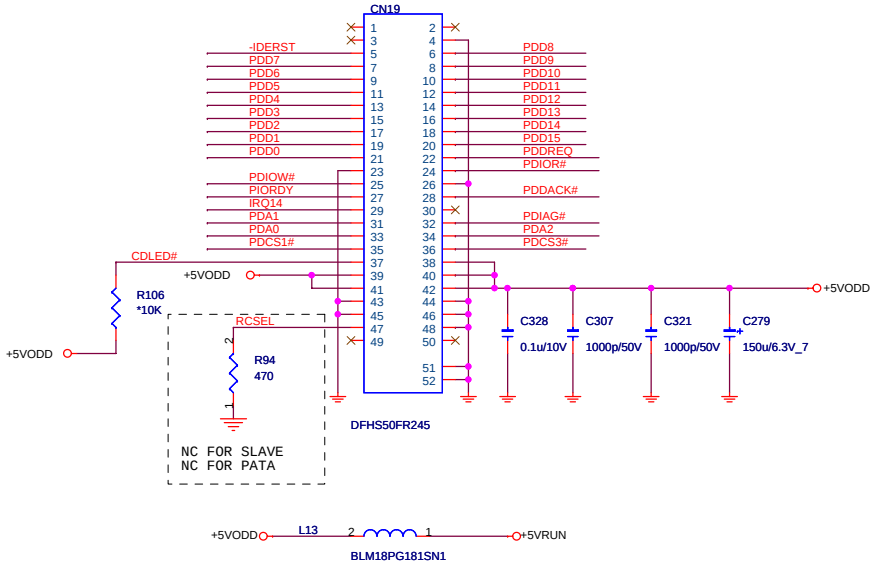




PATA HDD



ODD



FOR PATA HDD

CN19	NI
C730	NI
C729	NI
CN18	HDD CON
R517	NI
Q25	2N7002
Q26	2N7002
R513	10K
R512	0
R168	470

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Quanta Computer Inc.

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	SATA,PATA(HDD,ODD)	3B

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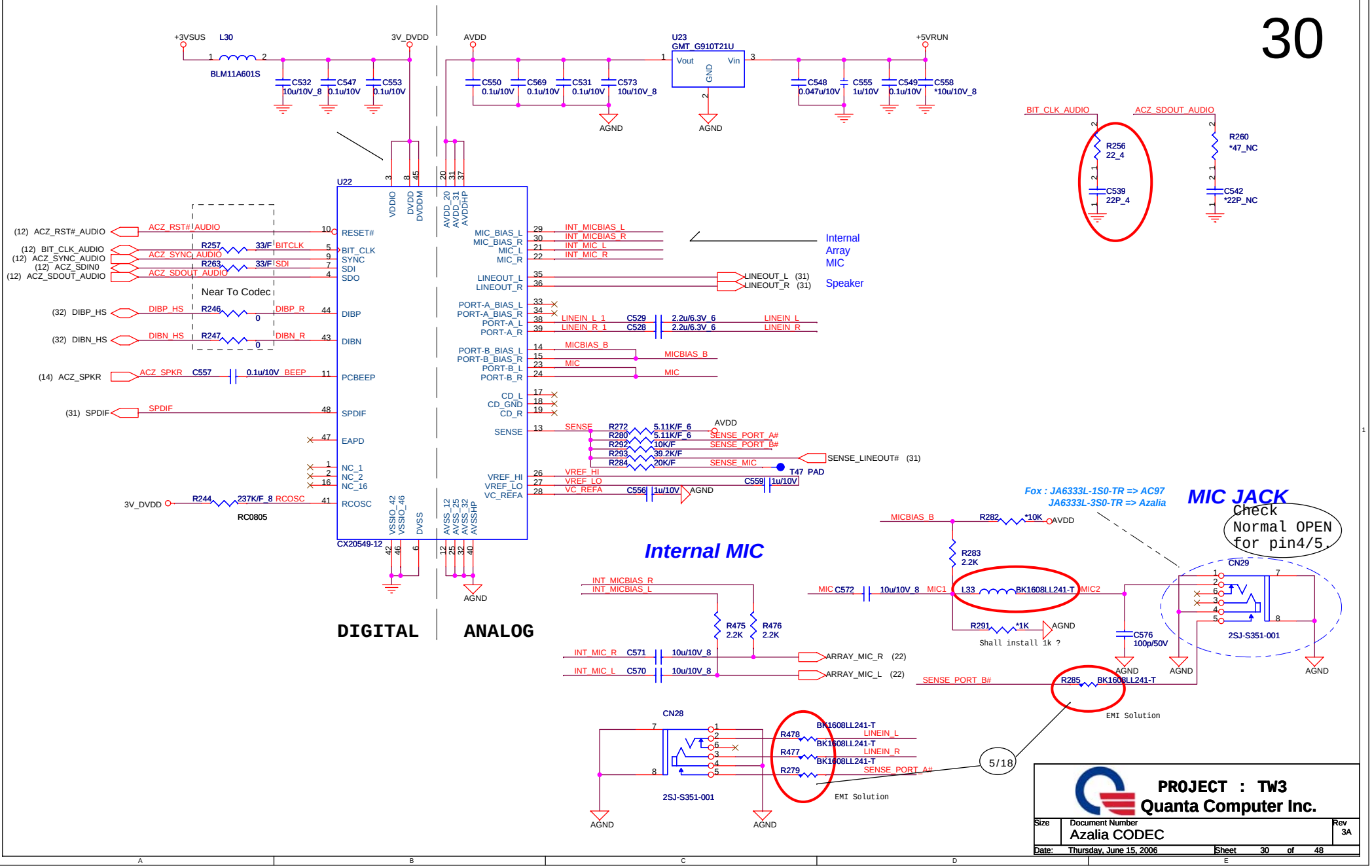

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Size	Document Number	Rev
	Azalia CODEC	3A
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Modify Library to QFN28-5X5-5-33P(Add thermal Pad) 04/06/2006 by Tony Huang

04062006

EAPD
low:mute

HEADPHONE OUT/SPDIF

GAIN	SPKR MODE	HP MODE
0	10.5	3
1	9	0

New add Pin29~31

Check Normal OPEN for pin4/5.

SPEAKER CON. BK1608HM121

3/9 Tony Huang

When Docking insert , disable BTL

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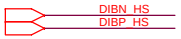
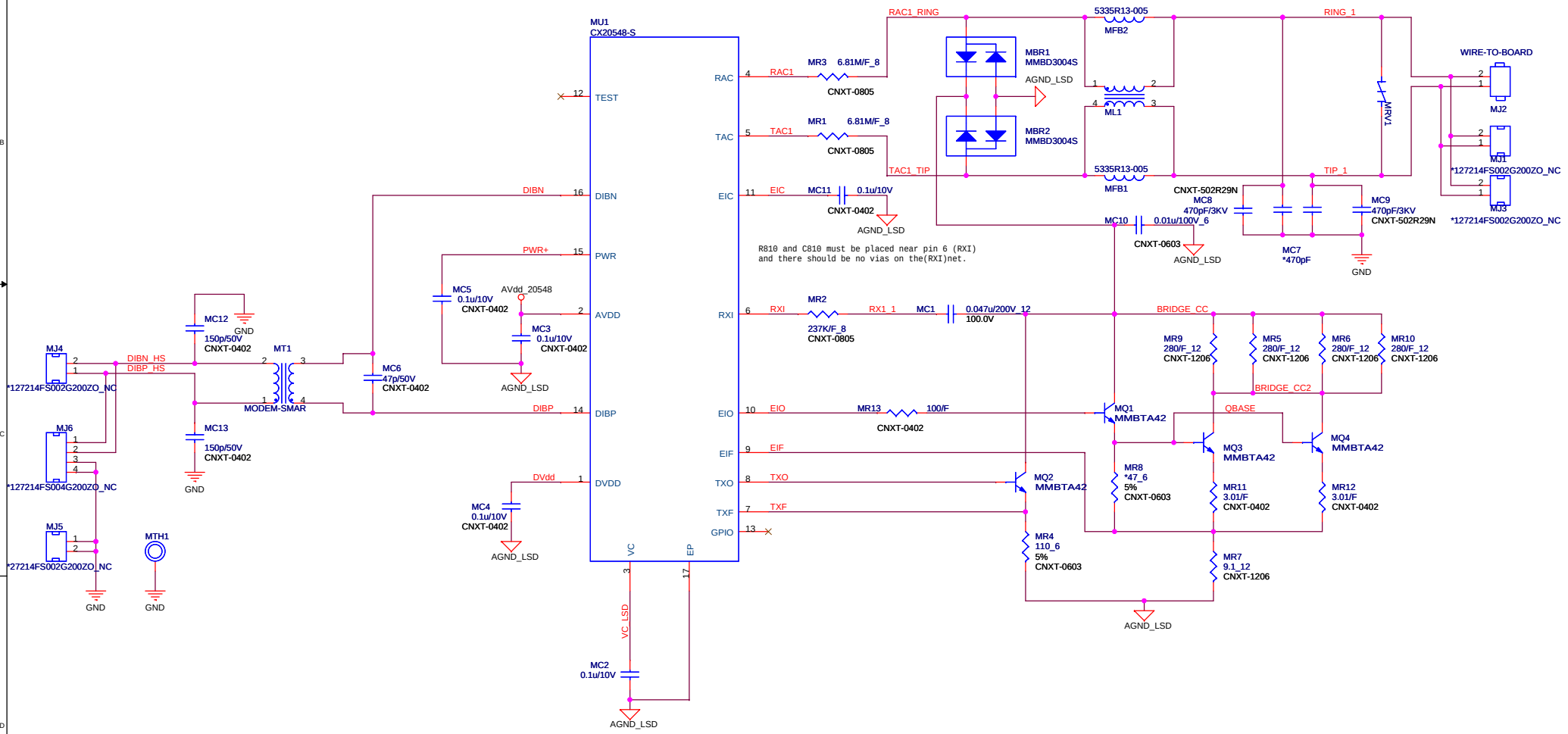
Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005

(30) DIBN_HS
(30) DIBP_HS





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	Conexant Modem	3B
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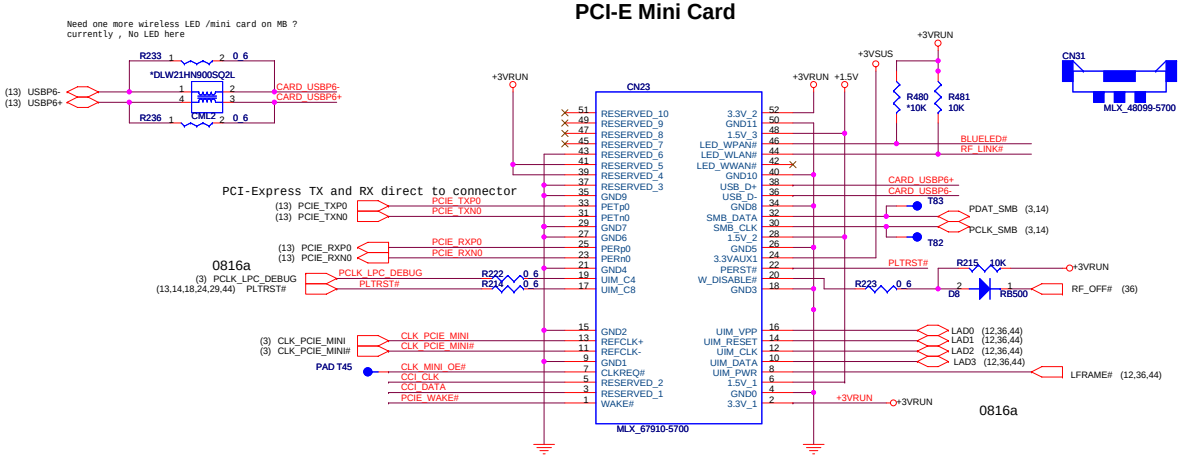
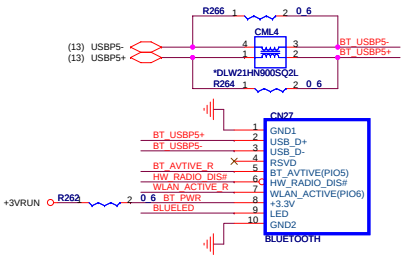
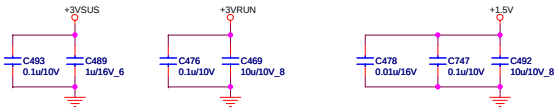
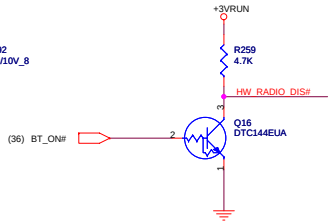
PCI-E Mini Card

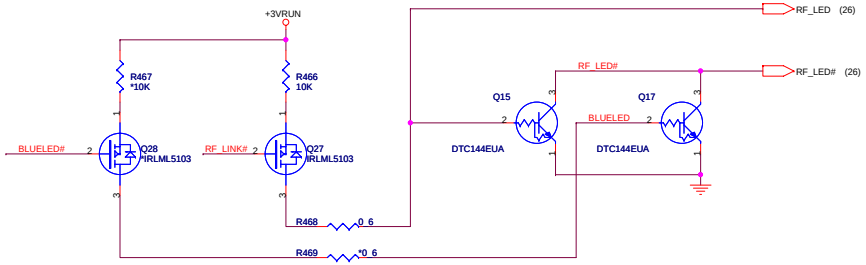


BLUETOOTH CONNECTOR

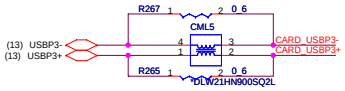


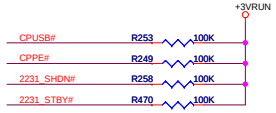


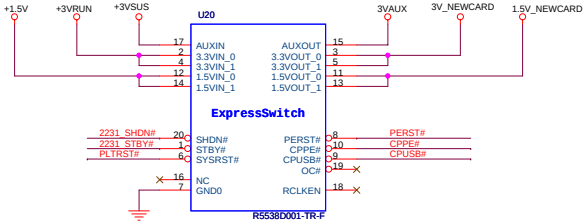


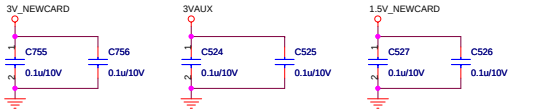


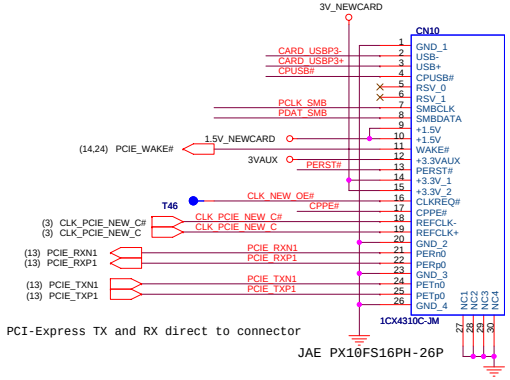
NEWCARD (PCIEXPRESS*1 + USB*1)

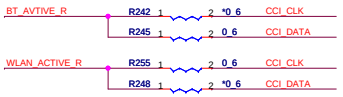












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	BT,NEW CARD,MINI PCIE	3B

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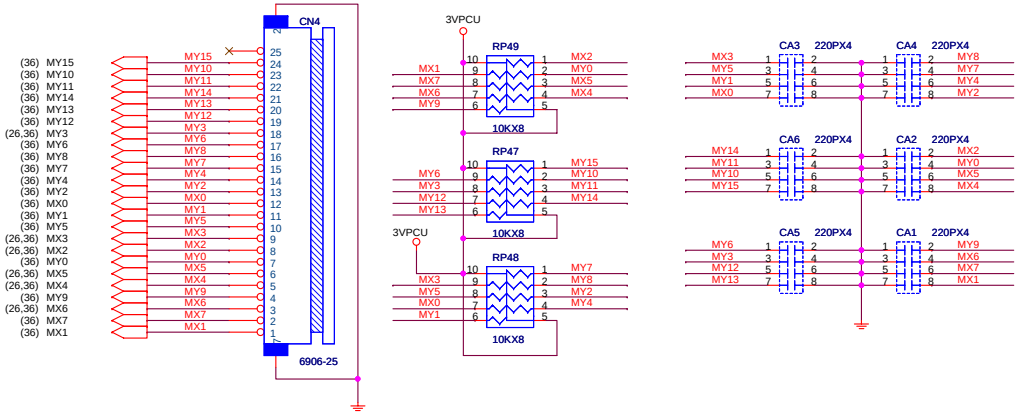
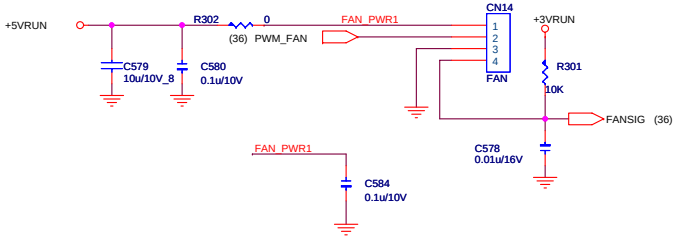
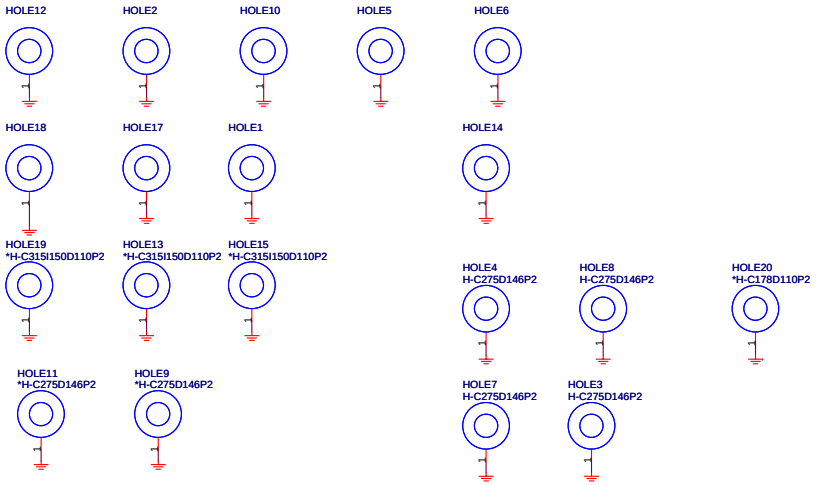
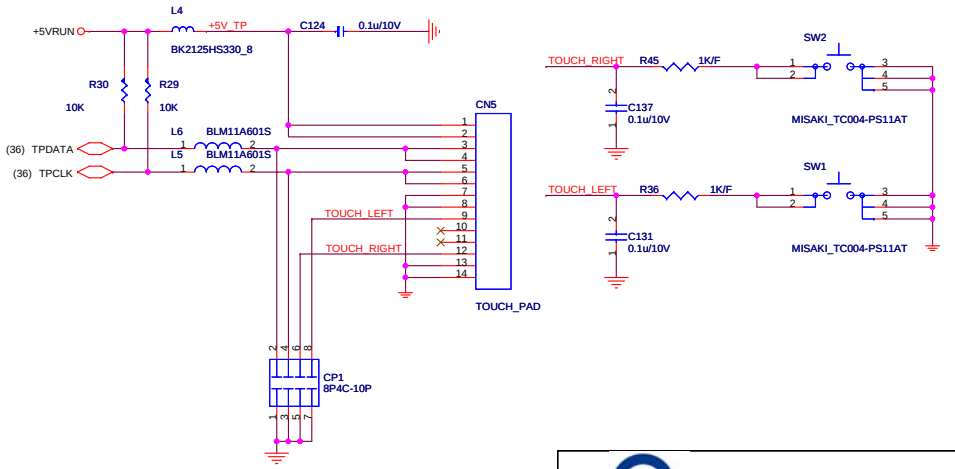
KeyBoard Interface







TOUCH PAD



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	T/P,FAN,KB	3A
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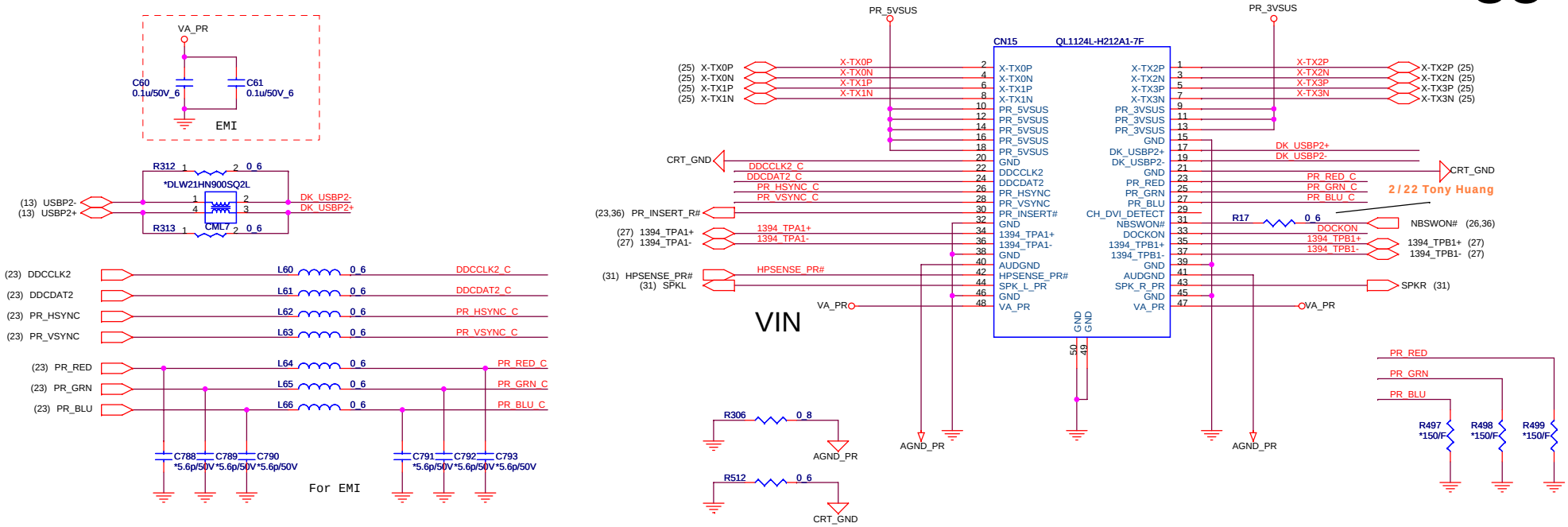
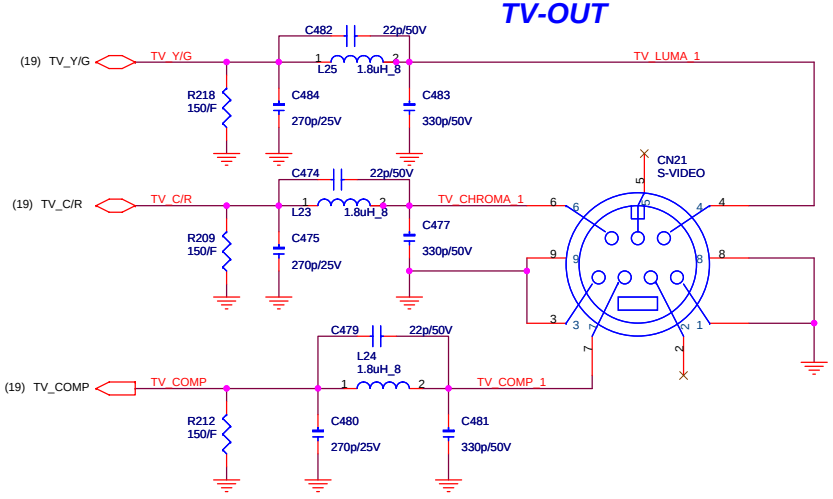
CABLE DOCKING CONNECTOR



TV-OUT



CX8PG181001 (180 ohm ,1.5A)

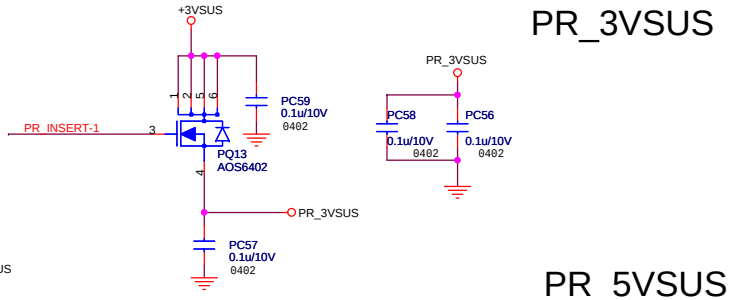
CH00606TB04 CH00606TB04

Intel CRB

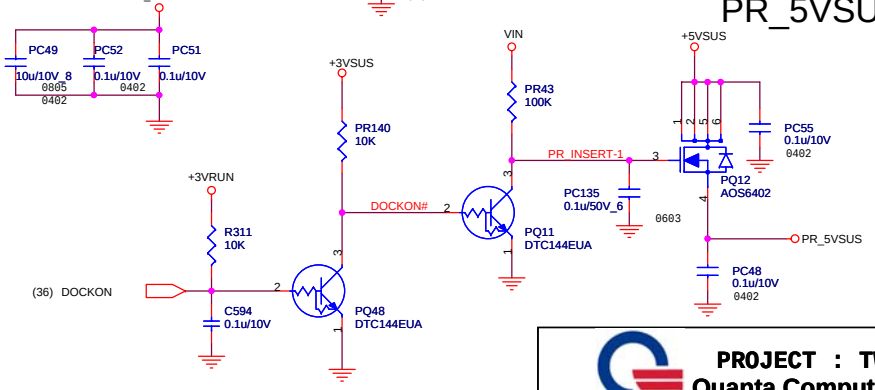
150 ohm@ 100MHZ
(100mA)

6pf 16V 6pf 16V

PR_3VSUS



PR_5VSUS



PROJECT : TW3
Quanta Computer Inc.

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	PORT REPLICATOR	3B
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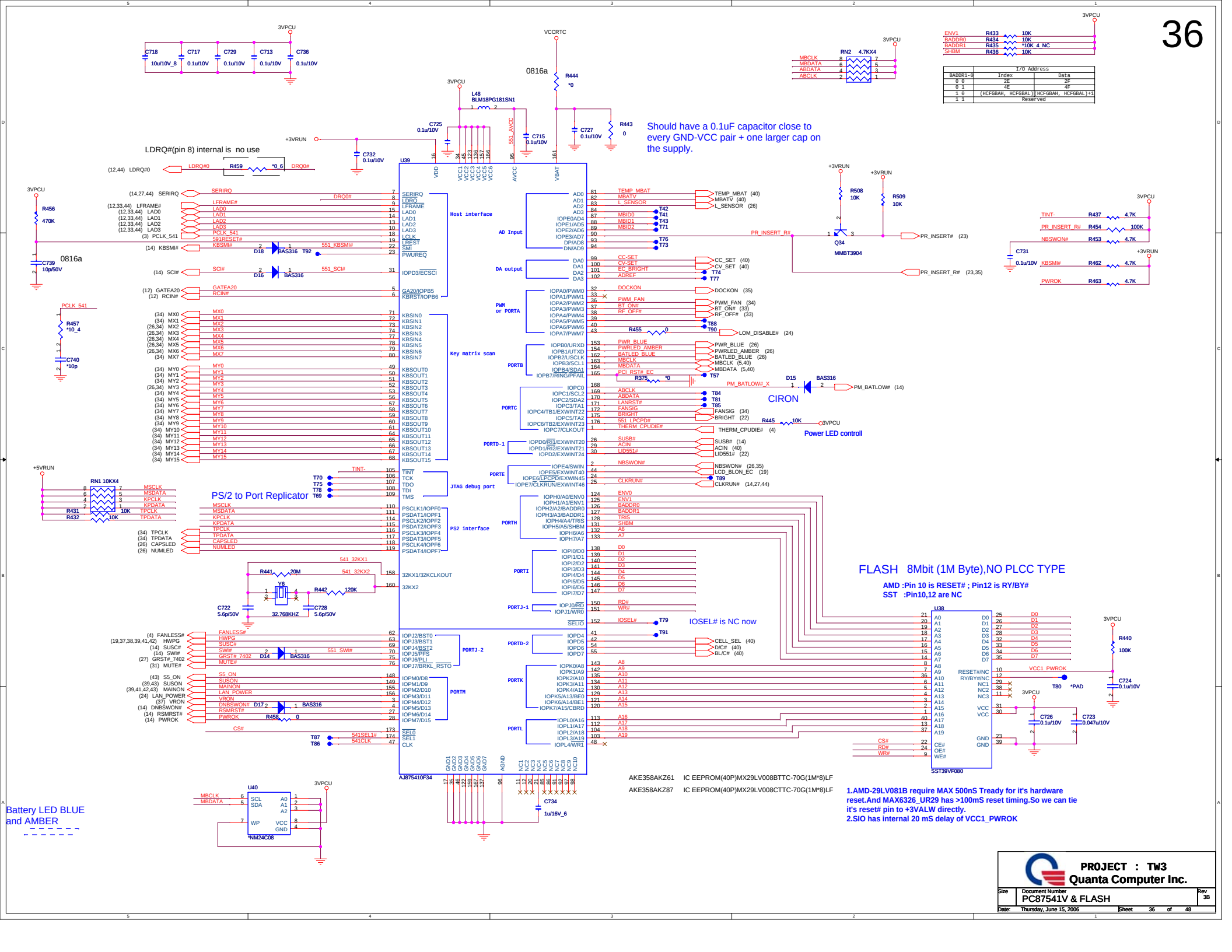

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Quanta Computer Inc.

Size	Document Number	Rev
	PC87541V & FLASH	3B

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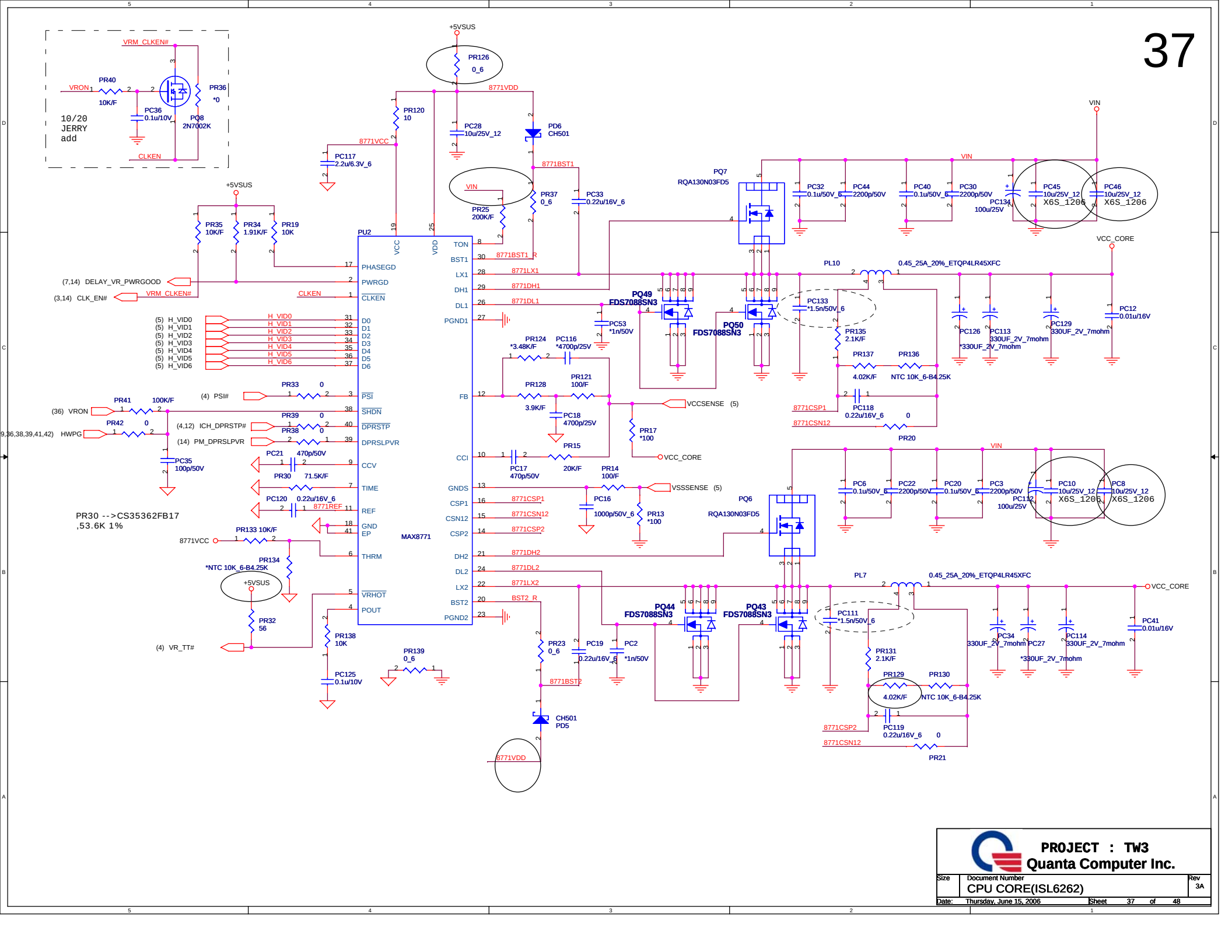

	PROJECT : TW3 Quanta Computer Inc.		
Size	Document Number CPU CORE(ISL6262)		Rev 3A
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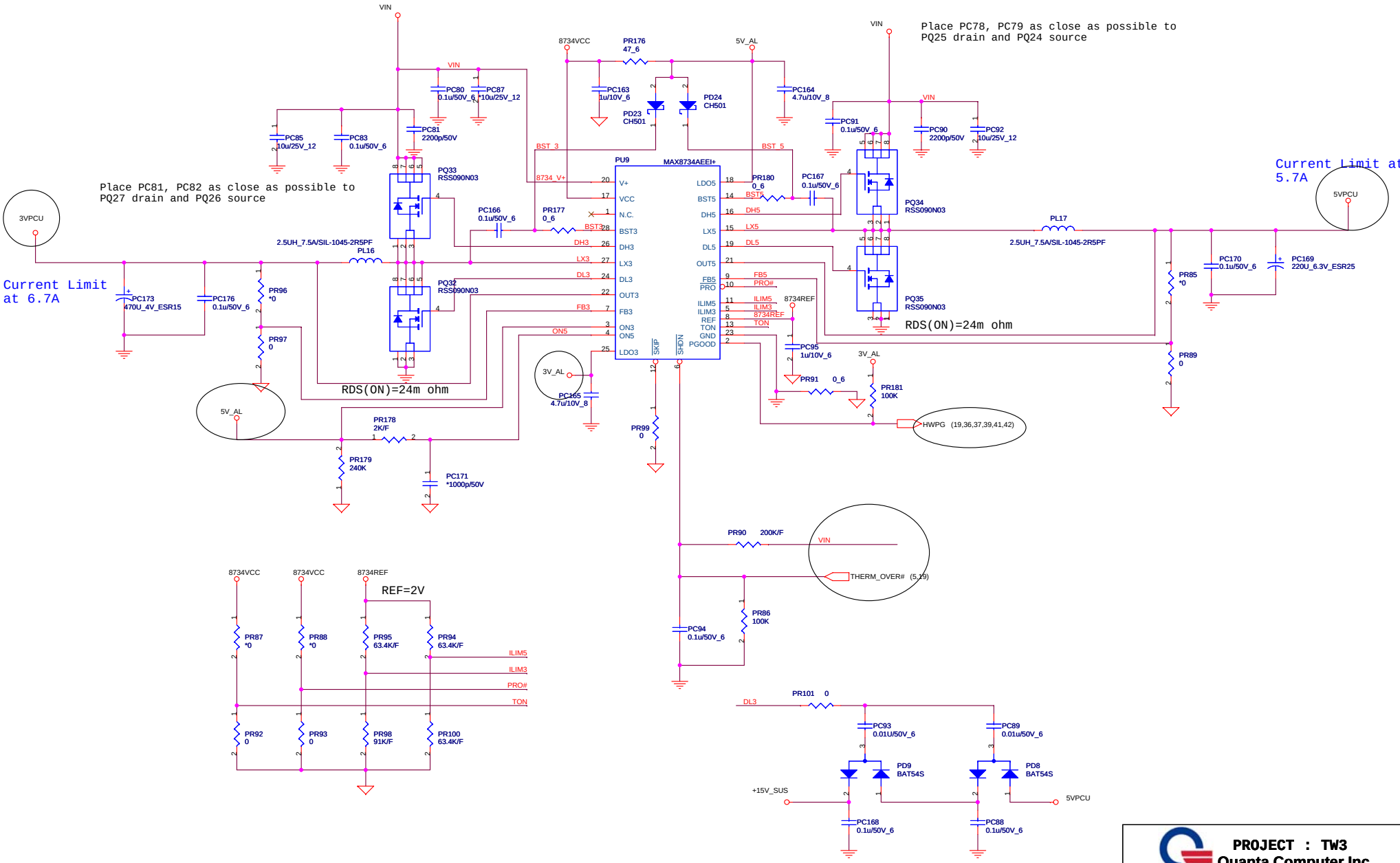

PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number	Rev
	5V/3.3V(TPS51120)	3A
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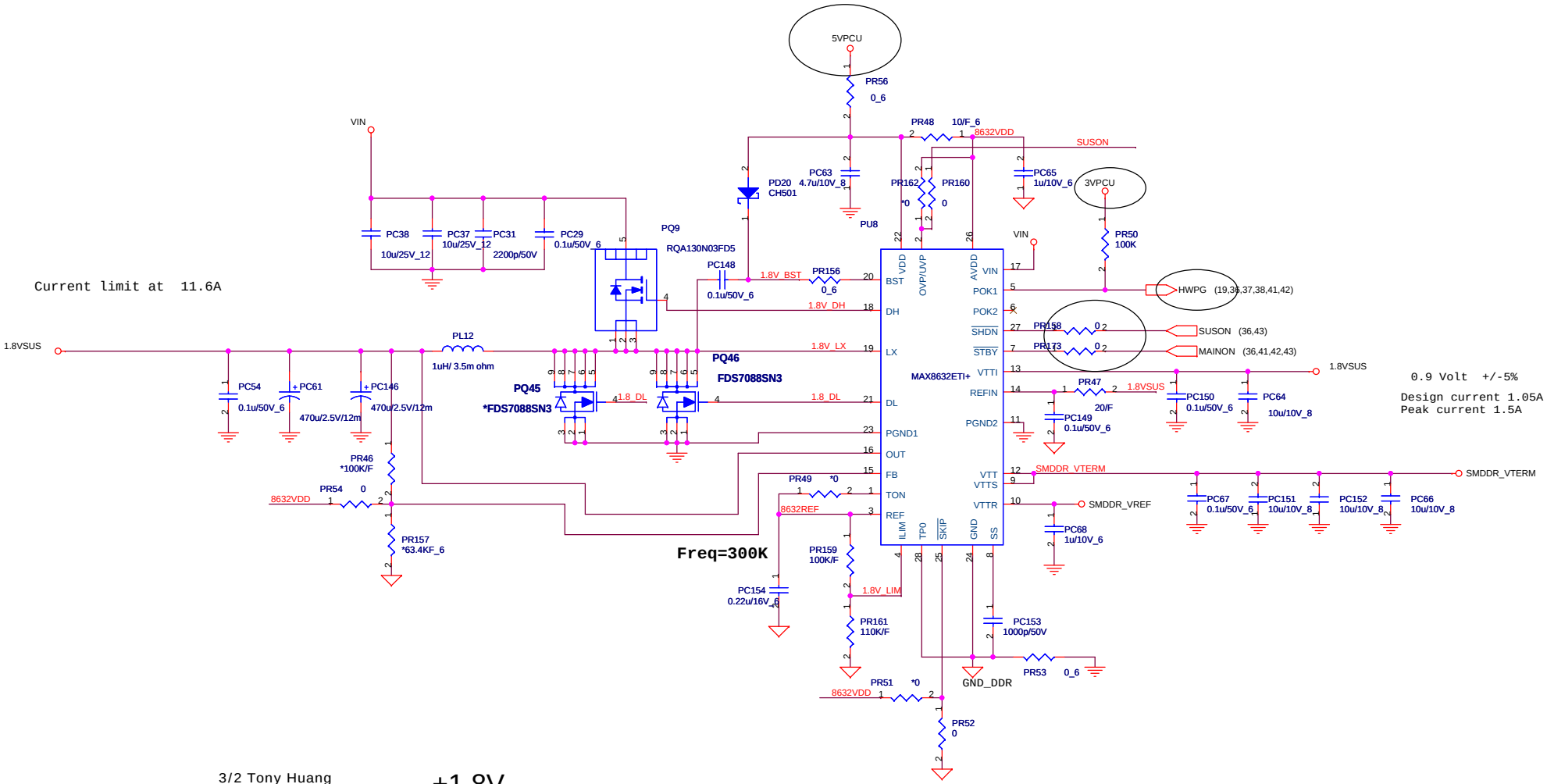

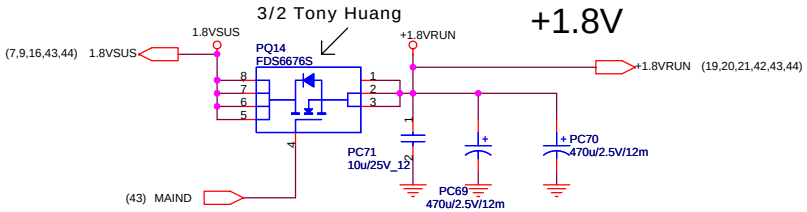

PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number	Rev
	1.8VSUS/+0.9TERM/+2.5VSUS	3A
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Iinput =(V CLS / V REF)*(0.075/ RS1)

ICHG =(V ICTL / V REFIN)*(0.075/ RS2)

CELL-SET
0 = 4 CELL
1 = 3 CELL

PU1 MAX8724

PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER	3A

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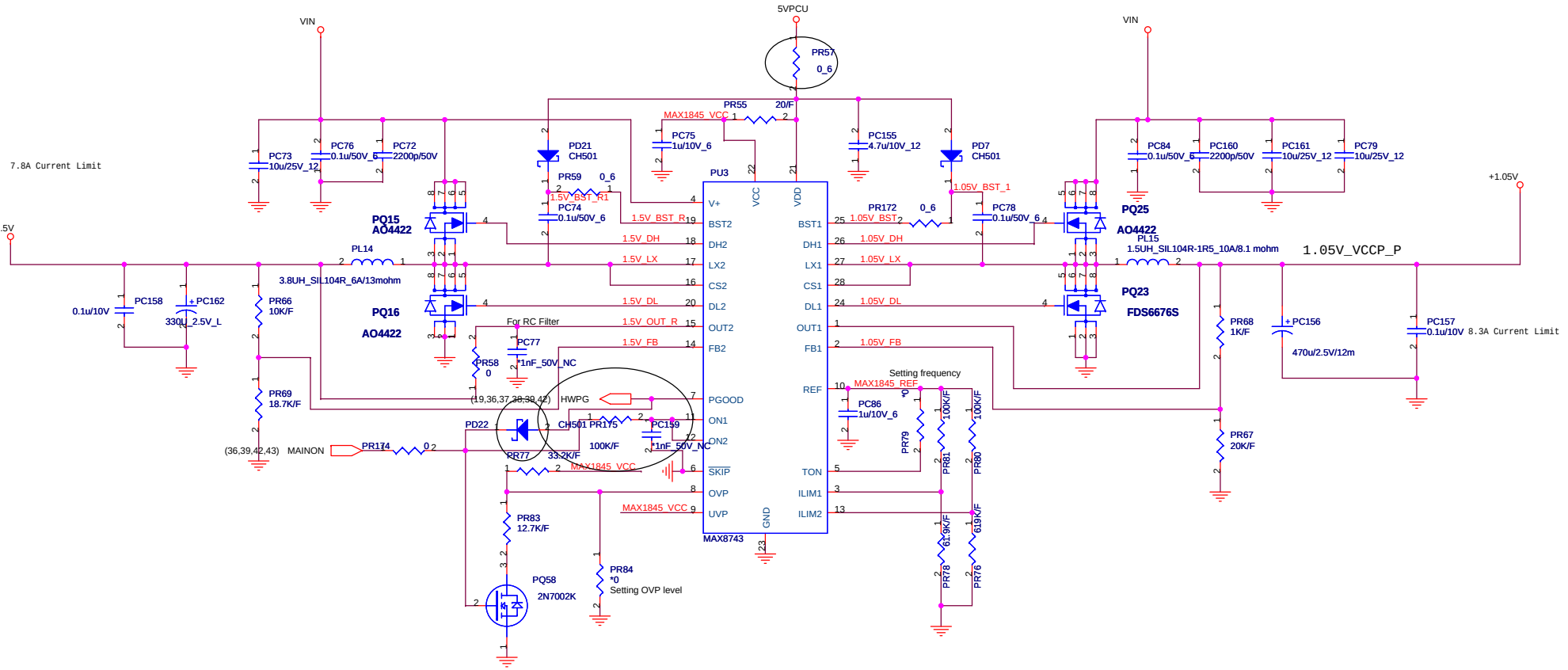
AO4422: Id= 11A, Rdson= 24m ohm, Qg= 19.8nC
FDS6676S: Id= 14.5A, Rdson= 7.25m ohm, Qg= 43 nC



PROJECT : TW3		
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	1.05V&1.5V	3B
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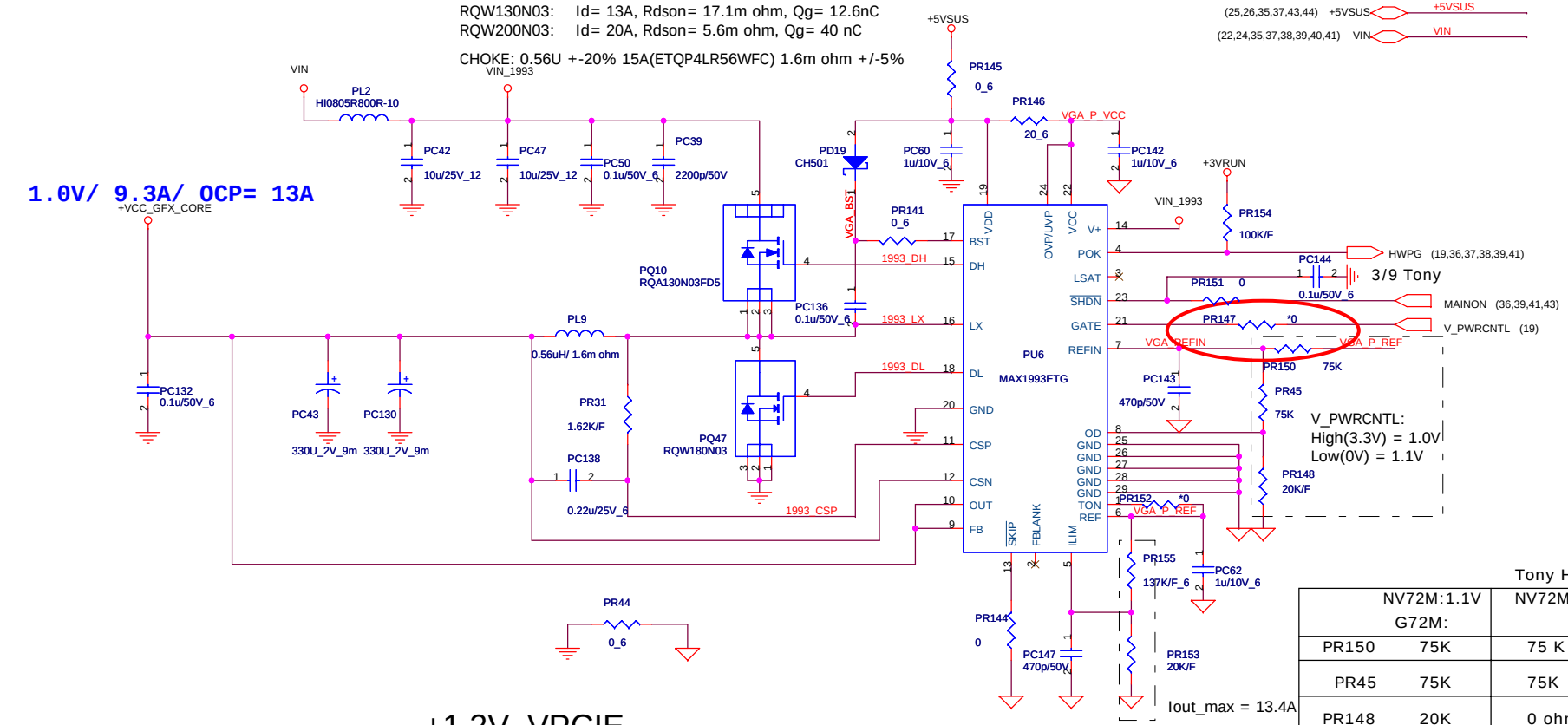
(13,14,25,30,33,35,43,44) +3VSUS +3VSUS
(25,26,35,37,43,44) +5VSUS +5VSUS
(22,24,35,37,38,39,40,41) VIN VIN

RQW130N03: Id= 13A, Rdson= 17.1m ohm, Qg= 12.6nC
RQW200N03: Id= 20A, Rdson= 5.6m ohm, Qg= 40 nC

CHOKE: 0.56U +-20% 15A(ETQP4LR56WFC) 1.6m ohm +/-5%

1.0V/ 9.3A/ OCP= 13A

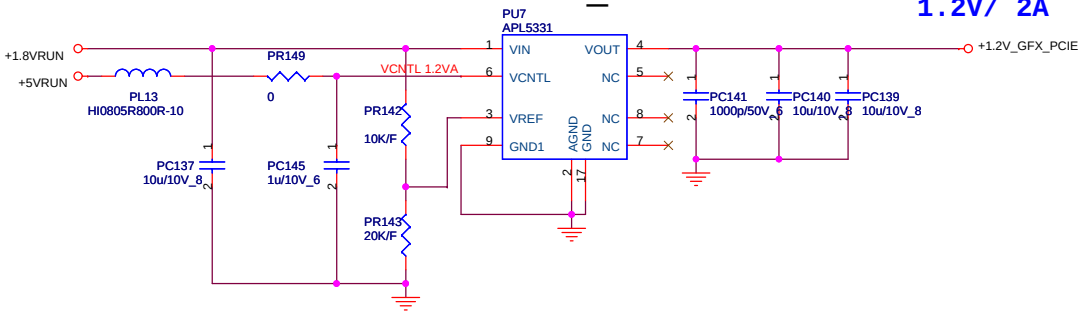


Tony Huang 3/2

	NV72M:1.1V G72M:	NV72MV:1.0V
PR150	75K	75 K
PR45	75K	75K
PR148	20K	0 ohm
PR147	NC	NC

+1.2V_VPCIE

1.2V/ 2A



PROJECT :	TW3
Quanta Computer Inc.	
Size	Document Number: VGA CORE
Rev	3A
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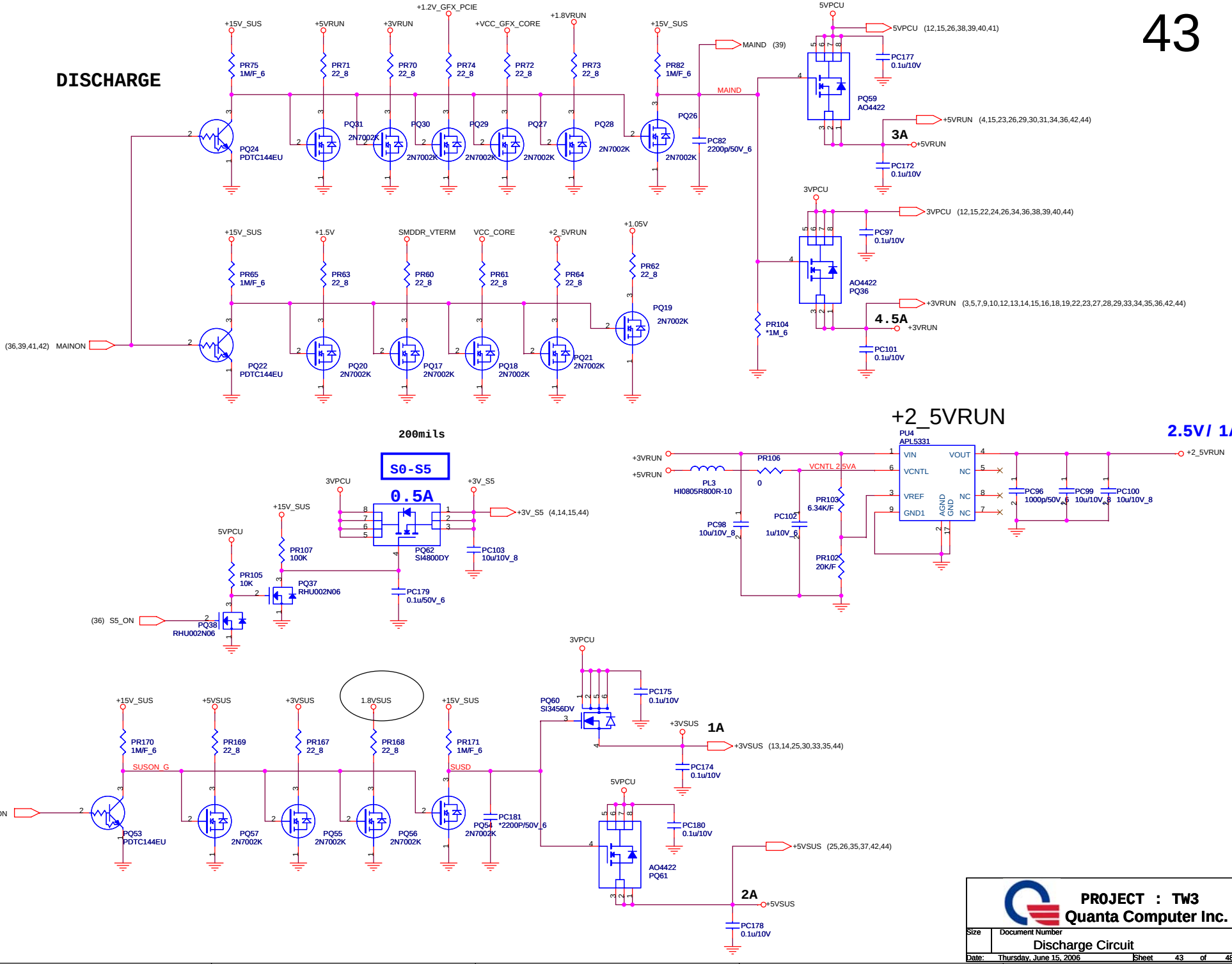
DISCHARGE



PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge Circuit	3B
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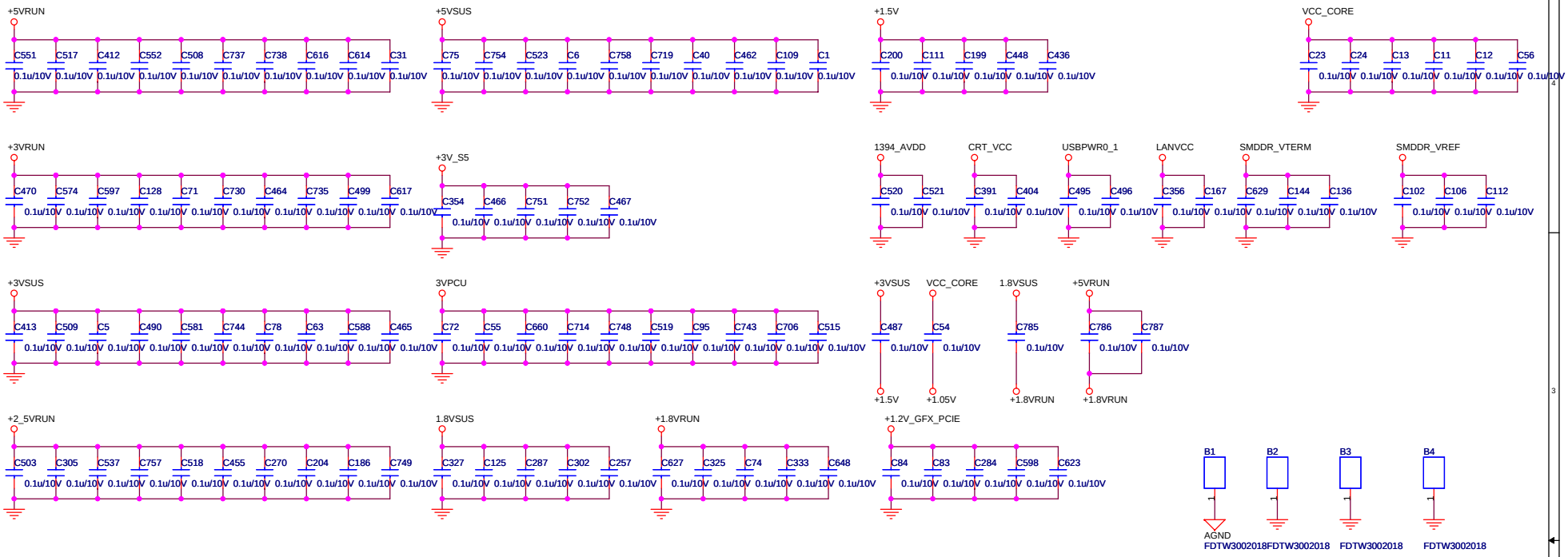
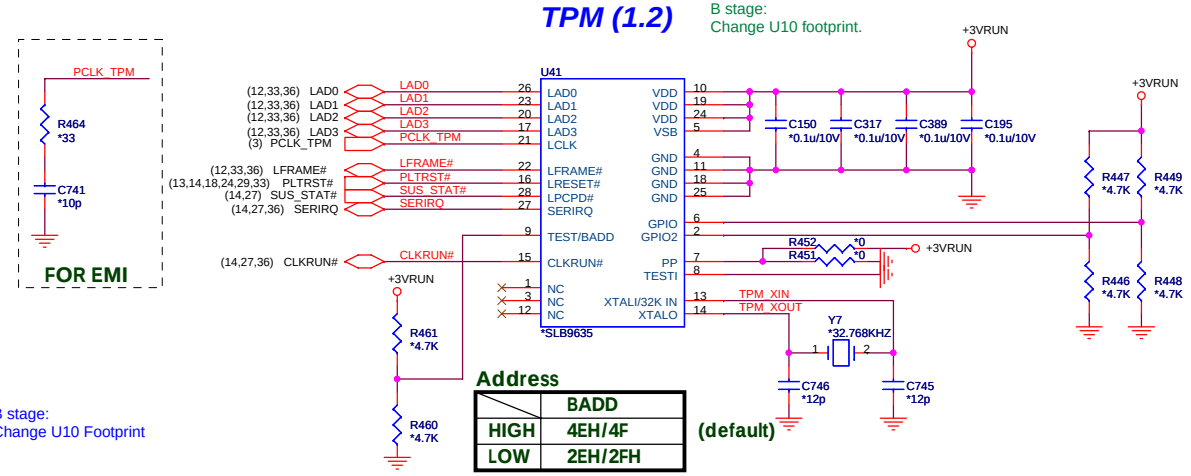


TPM (1.2)

B stage:
Change U10 footprint.

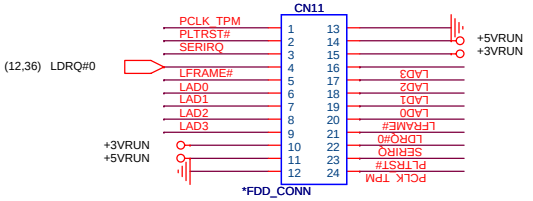


Address	BADD
HIGH	4EH/4F
LOW	2EH/2FH

(default)

B stage:
Change U10 Footprint

Debug Conn.



Size	Document Number		Rev
	EMI & TPM & Debug Conn		3A
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PROJECT : TW3
Quanta Computer Inc.

MODEL	DATE	Change Note	
TW3A		Page	Description
	B to 1223	Page 29	Change R472 to NI for SATA,install for PATA to solve sometimes ODD can't be detected and slow boot..
		Page 33	Add R481,R480 to solve WLAN LED light leakage.
		Page 3	Change R177 to install and pull low to set VGA clock to 100MHz.
		Page 19	Change R345 to install to solve back light can't enable.
		Page 29	Change R245 to NI for SATA,install for PATA.
		Page 14	Add R482,R483 for CRT/DVI option.
		Page 24	Change C645 to 10uF for LAN 1.2V per Marvell recommendation.
		Page 19	R377 to install,R362,R364,R365 to NI. (Set default to G72M)
		Page 30	3V_DVDD connect to +3VSUS to solve WOR.
	1223 to 1224	Page 32	Change MQ1,MQ2,MQ3,MQ4 to BA000420Z07 to solve MODEM low performance.
		Page 37	Delete short pad.
		Page 38	Delete short pad.PC92 change to install.
		Page 39	Delete short pad.
		Page 41	Delete short pad.
		Page 42	Delete short pad.PR45,PR150 change to 75K(CS37502FB04).
		Page 43	Delete short pad.
		Page 5	R19 change to NI for solving power-on shutdown.
		Page 34	HOLE,3,HOLE4,HOLE7,HOLE8 change to MBRW1003011.
		Page 40	PR110 change to CS+0158JL11.PR132 change to 24.9K.
		Page 37	PC34,PC113,PC114,PC129 change to CH733RM8831.
		Page 23	F1 change to DK100TPU028.
		Page 33	Q17 change to install for BT LED control.
		Page 34	Change CN4 footprint to "afn250-a2g1t-25p-l" for SMT issue.
		Page 26	Change CN1.4 connection to RF_LED.
		Page 33	Add NET RF_LED.
		Page 36	Delete NET TUCHLED.
		Page 31	Change C541,C546 to X7R for audio precision.
	1223 to 1226	Page 38	Change PC93,PD9,PC168 to install. Delete NET 10V.
		Page 41	Change NET 10V to +15V_SUS.
		Page 26	LED2,LED3 change to dual color type(cost down and unify brightness and color).
		Page 12	Reserve C784 on THERMTRIP for ESD.
		Page 35	Reserve R497,R498,R499 for TW2 PR.
		Page 33	Delete RP45,RP46,R210 for layout problem.
	1226 to 1227	Page 33	Change CN23 to Molex (same as SW1). Add CN31 PCIE latch.
		Page 44	Add EMI spring B1,B2,B3.
		Page 32	Install MC8,MC9 for EMI.
		Page 12	Change C459 TO 22pF for EMI.
		Page 31	R479,R281,R295 change to install for EMI.
	1227 to 1228	Page 44	Add B4,C785,C786,C787 for EMI.
		Page 19	Reserve R504,R505,R506,R507 for DVI EMI.
		Page 3	Change Y1 P/N to BG614318081(CL=20pF) for solving system time delay issue.
		Page 23	Change C694,C701,C703 to NI for signal quality.
		Page 36	RN2 change to 4.7K for IIC signal quality.
		Page 30	C528,C529 change to 1uF/10V X5R for audio precision.
		Page 35	Add L60~L66,C788~C793 for EMI.
	1227 to 1230	Page 26	Change CN9,CN12 P/N to DFHS04FRE80.
		Page 36	Delete D13, add R508,R509,Q34 for PR leakage current. R454 change to 100K.

Change Note

MODEL	REV	Page	Description
TW3A			
	1230 to 0102	Page 38	PC173 change to 470uF.
		Page 39	PC66 change to install.
		Page 42	PR153 change to 20K.
		Page 41	PD7,PD21,PD22 change to CH501.
		Page 37	PD6,PD5 change to CH501.
		Page 42	PQ47 change to RQW180N03.
		Page 26	CN12,CN9 USB connector change to DIP type.
		Page 29	CN25 pin25,26 and CN24 pin47,48 disconnect to GND.
		Page 23	CN6 pin27,28 disconnect to GND.
		Page 34	SW1,SW2 P/N change to DHP00FC1G16.
		Page 36	Change R454 to 100K,R508,R509 to 10K.
	0102 to 0103	Page 4	R101,R97,Q11 change to install.
		Page 6,7,8,9,10,11	Change U32 P/N to AJSL8Z40T26.(945PM)
		Page 12,13,14,15	Change U36 P/N to AJSL8YB0T12.(ICH7M)
		Page 37	PR128 change to 3.9K.
	0103 to 0105	Page 45,46	Update change list.
		Page 27	Change J1 P/N to DFHS04FRE47.
		Page 35	Change CN15 to install and P/N to DFHS48FR001
		Page 44	Change B1,B2,B4 P/N to FDTW3002018.
		Page 36	U38 P/N change to AKE35ZAKK17.
		Page 42	PR45,PR150 P/N change to CS37502FB12.
	0105 to 0111	Page 30	Change C528,C529 to 2.2uF/6.3V for audio precision.
C1 TO C2	0111 to 0119	Page 19	Change R26 to 0 ohm and change connection to THERM_OVER#.
		Page 23	Q21 mirror vertical.
		Page 23	Add C794~C799, L67~L69 for EMI.
		Page 23	L46,L44,L42 change to 0 ohm. C700,C702,C705 change to NI for EMI.
		Page 32	Change MR5,MR6,MR,MR10 to 280ohm. Add MR11,MR12,MR13. Change MR8 to NI.
		Page 35	R17 change to install.
		Page 35	CN15.21,22 change to CRT_GND. Add R512 for EMI.
		Page 35	Change D1 to page23 and its connection and to NI.
		Page 41	PL14 P/N change to DC-38600001.
		Page 43	PQ59,PQ61,PQ36 P/N change to BAM44220002.
		Page 36	RN2 P/N change to CJ247084N25.
		Page 26	LED4 P/N change to BEBL0002Z62. LED1~3 P/N change to BEAB0013ZA1.
		Page 33	CN10 P/N change to DFHS26FR489.
	0119 to 0120	Page 14	Change R368 to install,R366 to NI to set w/ docking.
		Page 27	Change D7 to install to solve 7402 does not work.
		Page 19	Delete R410,R413,R417 for EMI layout.
		Page 23	Correct CN6 C1~C4 pin define.
		Page 23	Reserve Q37,Q38,RP56,R513,R514 for DVI disable when docking attach.
		Page 29	CN25 footprint change to "SATA-C16647-122A4-B-22P-R-V" for SMT issue.
C2 TO C3	0120 to 0209A	Page 25	LAN active/link LED change to +3VSUS.

MODEL	DATE	Change Note	
		Page	Description
TW3A	0209 to 0222A	Page 23	**(1)** CN20 pin 12,15 change connect to DVI_DDCDAT,DVI_DDCCLK **(In C1 was connect to DDCCLK2,DDCDAT2)**
			(2) R150,R159,Q37,Q38,RP56 Change to install for DVI,CRT I2C,D1 change to NI
			(3) Change L67,L68,L69 P/N from CX8BB121002 to CX8BB470007
C2 to C3			**(4)** Change C794,C795,C796,C797,C798,C799 P/N from CH01806JB07 to CH01006JB08
		Page 27	**(1)** Change R208 pin1 contact to +3VRUN
			Change R208 P/N to CS31002JB28,C473 change to CH4102K1B03 ,D7 change to NI.
		Page 34	**(1)** RP47,RP48,RP49 change to CJ3100A8N21(meet Rohs)
		Page 42	**(1)** Change PR147 to NI
Production	0222A to 0407A	Page 26	**(1)** Change CN9,CN12 layout footprint to usb-020133mr004s566zl-c-h
		Page 31	**(1)** Change U21 layout footprint to QFN28-5X5-5-33P(add thermal Pad)
	0407A to 0510	Page 23	**(1)** Change C794~C796 to 6.8PF(CH-6816TB05)
			(2) Change C797~C799 to 33PF(CH03306JB04)
			(3) Change L67,L68,L69 to BLM18BA750SN1D,75 0.3A(CX8BA750006)
	0510 to 0523	Page 12	**(1)** Change R186 from CS03902JB21 to CX5LL241002 , C459 from CH02206GB02 to NI
		Page 19	**(1)** Change R504~R507 from CS11502FB21 to CH01006JB08
		Page 27	**(1)** Change EB1,EB2 from NI to DC09004A014 ,R286~R289 from CS00002JB38 to NI
		Page 30	**(1)** Change R477,R478 from CS03902JB21 to CX8LL241008,R279,R285 from CS00003J951 to CX8LL241008,
			L33 from CX221T05009 to CX8LL241008
			(2) Change R256 to CS02202JB22,C539 to CH02206GB02*R256 from NI to CS02202JB22,C539 from NI to CH02206GB02
		Page 31	**(1)** Change R268,R278 from CS03303J941 to CX8LL241008
			(2) Change C564 from NI to CH11006F909

PROJECT : TW3
Quanta Computer Inc.

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	Change Note	3A
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A. G72M to G72MV

1. change P/N to G72MV (AJ073000T14)
2. Set VGA core to 1.0V fix.
3. Change PCI_DEVID.

B. VRAM 128MB to 64MB

1.follow config table to set RAM_CFG.

2.Change VRAM P/N to HYNIX.

3.VRAMx2

C. LAN GIGA to 10/100.

1.Change LAN chip to 8038(AJ080380000).

2.Change Rset resistor.

3.Change transformer.

D. SATA to PATA

1.Set ODD to slave.

2.Set HDD to master.

3. Remove SATA conn.

4. Add PATA conn.

5. Change board ID to PATA.

6. Install resistor to connect ODD and HDD LED.

7. NI resistor of SATA LED.

E. docking to no docking.

1.Set board ID4 to low.